

ZSA MB Schematic Document

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2018.07.26

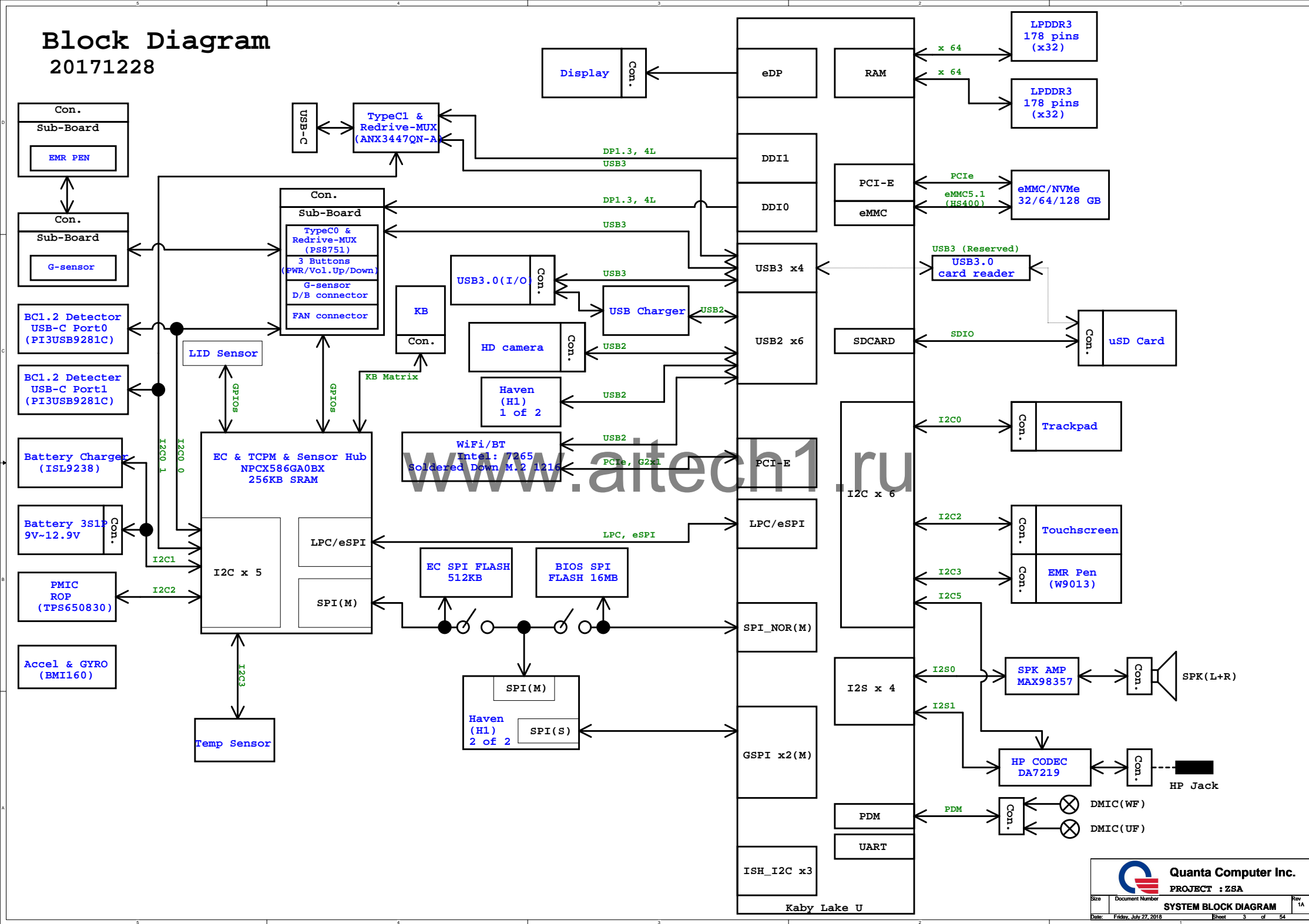
TABLE OF CONTENT

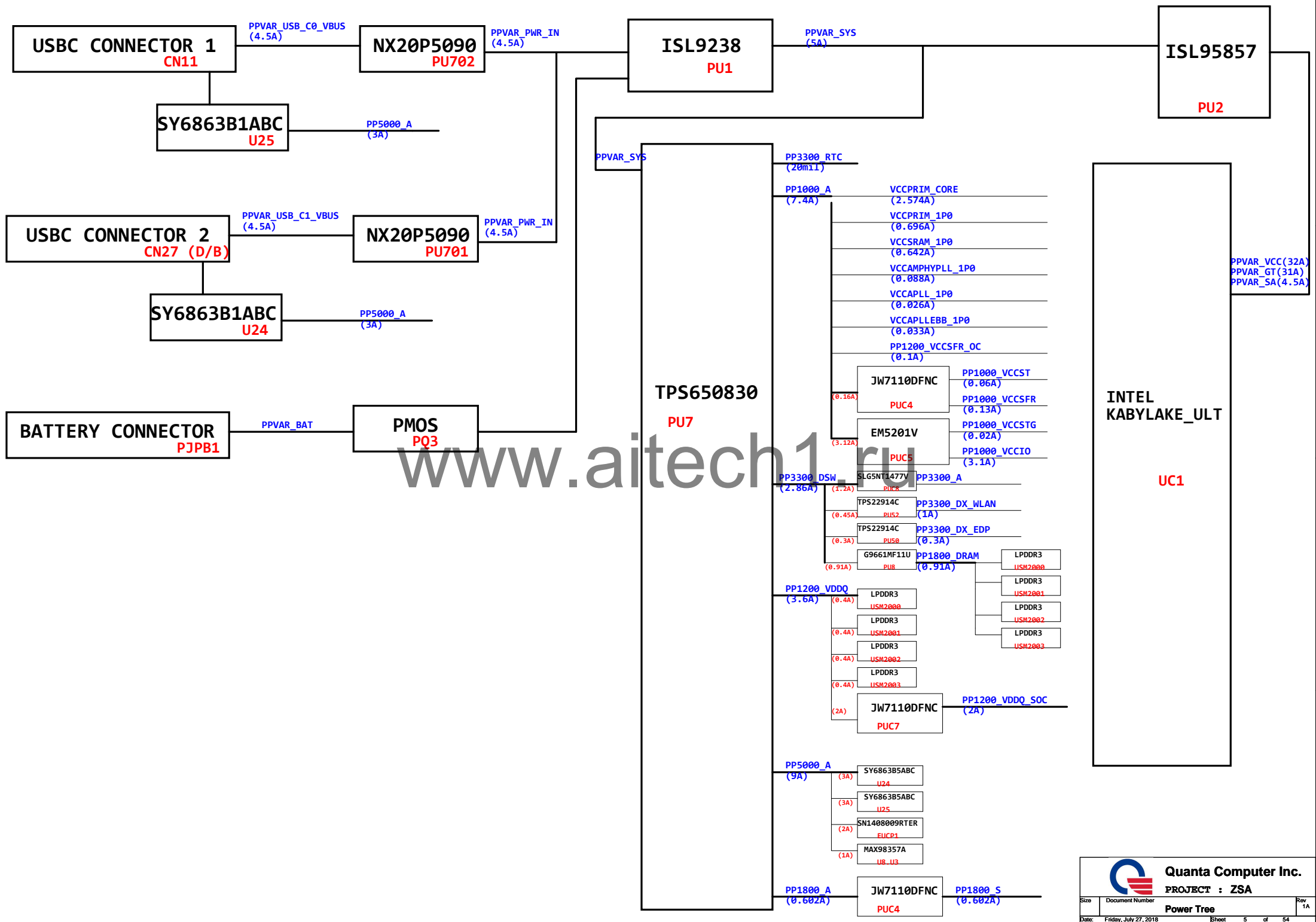
Trackpad/Thermal

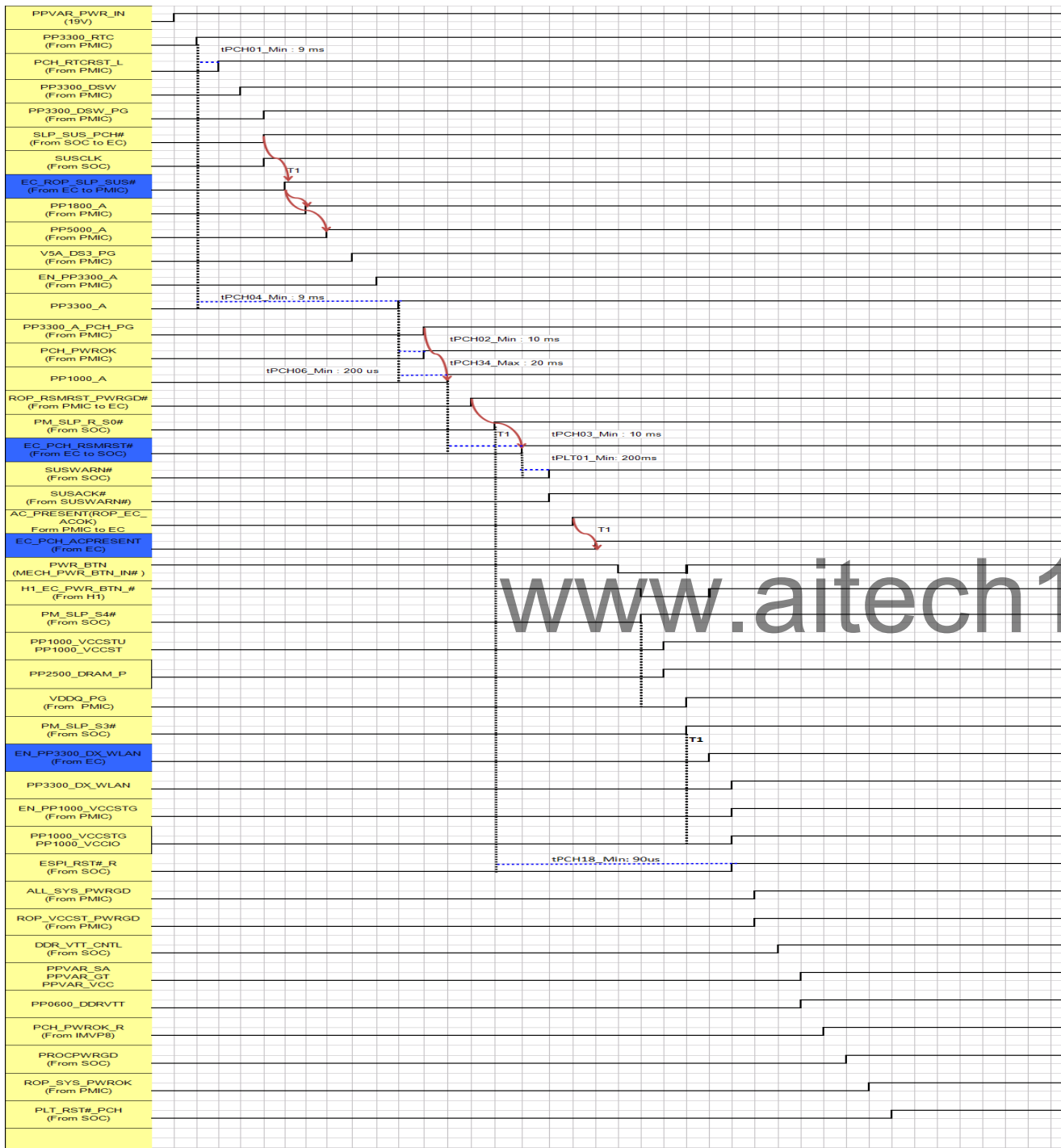
GMR/Srew

SHEET NO.	SHEET NAME	PAGE	TITLE
1	Cover Page	28	eDP / TOUCH / DMICs / CCD
2	TABLE OF CONTENTS	29	BLANK
3	BLOCK DIAGRAM	30	WLAN
4	Notes List	31	USB TYPE-C P0 /SD/SR
5	Power Map	32	USB TYPE-C P1
6	Power sequence	33	PCB, Screw, CLIP
7	SKU PLAN	34	USB Type-A
8	KBL-U(DDI/MISC/XDP/EDP)	35	HIBERNATE WAKE SOURCE
9	KBL-U(DDR3)	36	Trackpad/Thermal
10	KBL-U(SPI/I2C/SMB/Strapping)	37	KB/KB Backlight
11	KBL-U(I2S/DMIC/eMMC)	38	BLANK
12	KBL-U(CLK/GPIO)	39	INAs
13	KBL-U(PCIE/USB/SATA)	40	LOAD SWITCHES
14	KBL-U(POWER)	41	BLANK
15	KBL-U(POWER)	42	PWR AC/DC CONN/OTP
16	KBL-U(POWER/SVID)	43	PWR CHARGER
17	KBL-U(GND)	44	PWR PMIC-TPS650830(1of2)
18	KBL-U(RSVD)	45	PWR PMIC-TPS650830(2of2)
19	LPDDR3 CHANNEL A	46	PWR NVMe
20	LPDDR3 CHANNEL B	47	PWR IMVP8(1of3)
21	SPI EC ROM	48	PWR IMVP8(2of3)
22	SERVO	49	PWR IMVP8(3of3)
23	H1 SECURE	50	BLANK
24	EC(NPCX586GA0BX)	51	BLANK
25	eMMC / NVME	52	PWR ROP
26	HP AMP DA7219-02VBA	53	Addition Page
27	SPEAKER AMPS	54	Change List

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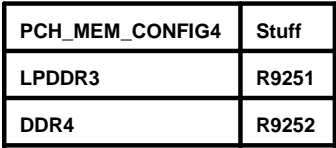


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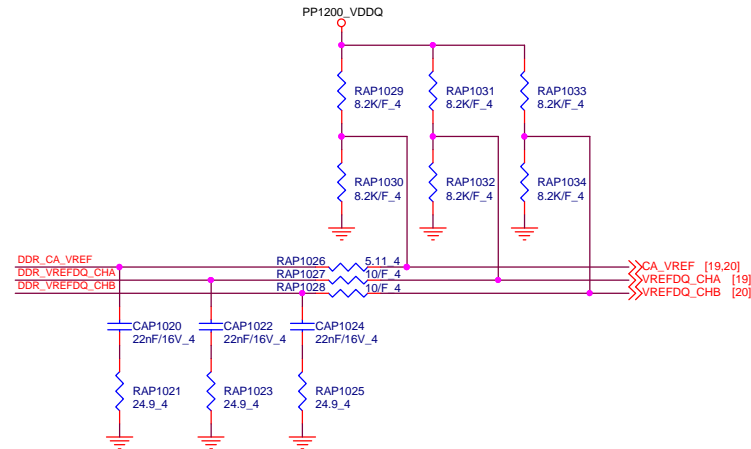
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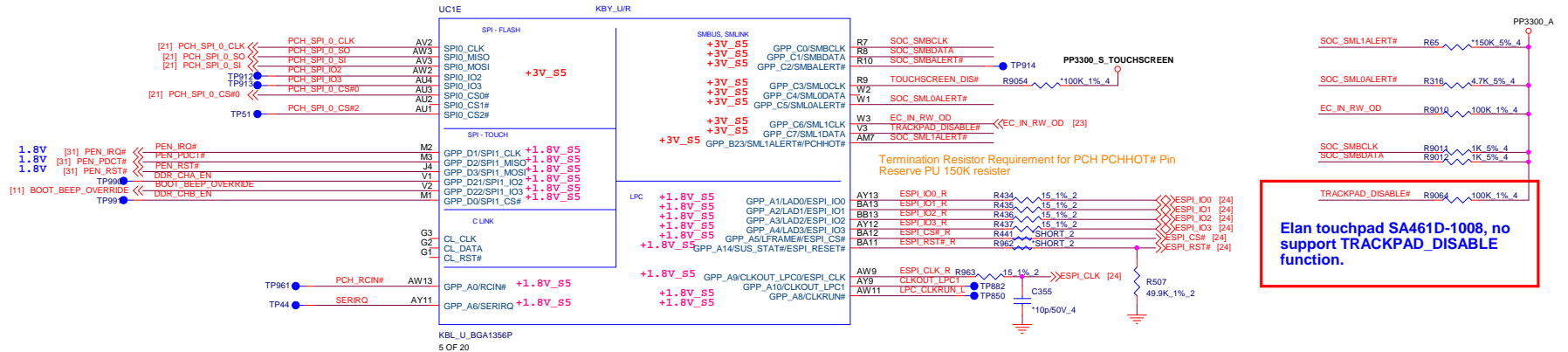
Size	Document Number	Rev
	SKU PLAN	1A
Date:	Friday, July 27, 2018	Sheet 7 of 54

08

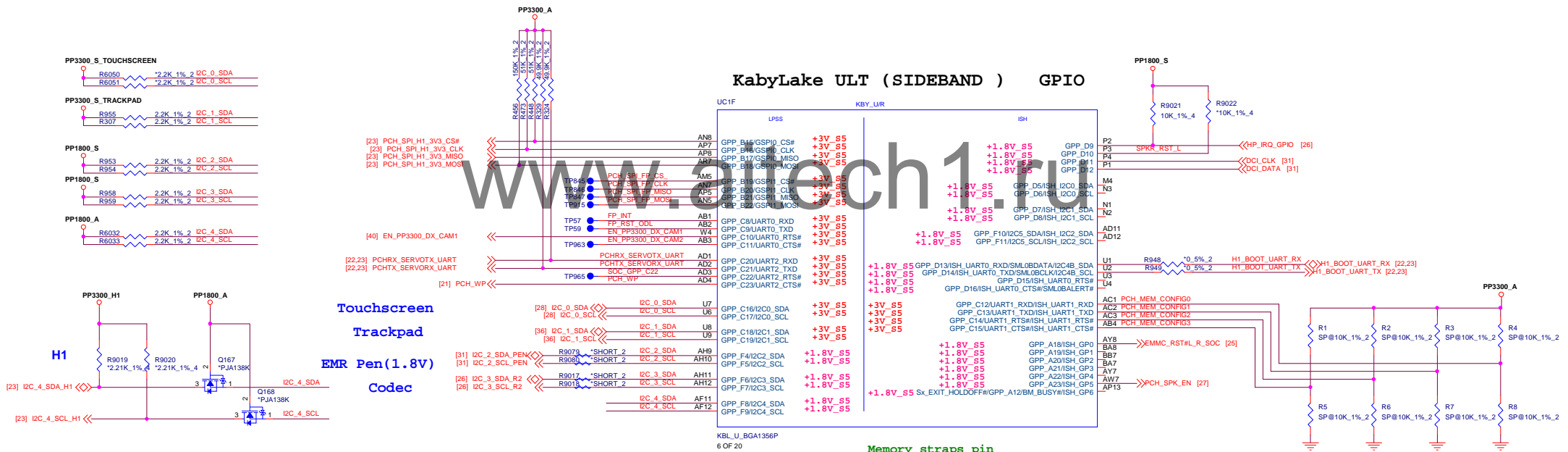


UC1C KBL_U/R





KabyLake ULT (SIDE BAND) GPIO



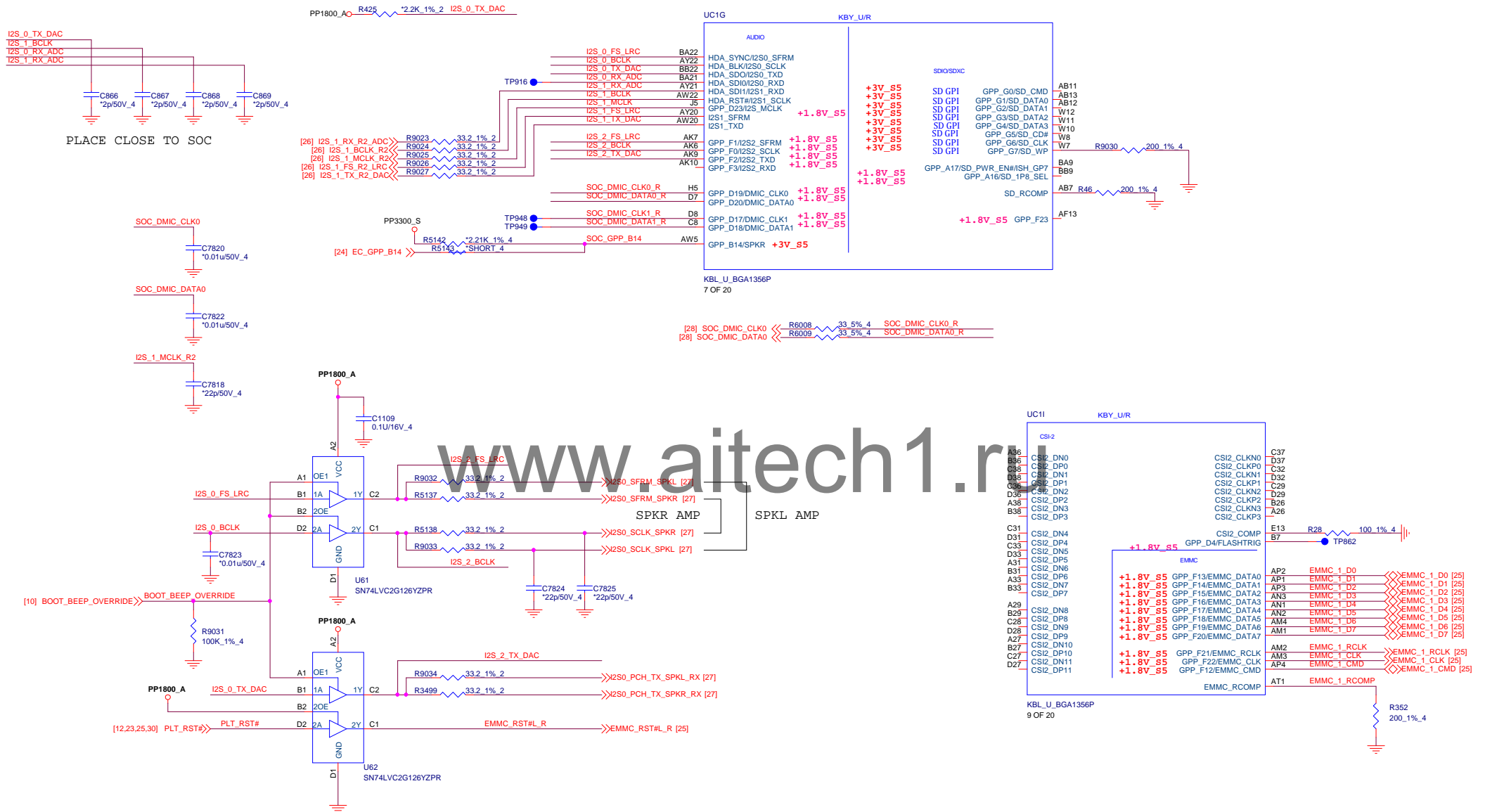
STRAPS ON THIS PAGE

Pin Name	FUNCTION	INTENT
GPP_B_23/SML1ALERTB#	IPD = EXI BOOT STALL BYPASS DISABLE PU = EXI BOOT STALL BYPASS ENABLED	DISABLE
GPP_B18/GSPI0_MOSI	IPD = DISABLE NO REBOOT MODE PU = ENABLE NO REBOOT MODE	DISABLE
GPP_C2/SMBALERT#	IPD = DISABLE TLS CONFIDENTIALITY PU = ENABLE TLS CONFIDENTIALITY	DISABLE
GPP_B22/GSPI1_MOSI	IPD = BOOT FROM SPI PU = BOOT FROM LPC	SPI
GPP_C5/SML0ALERT#	IPD = LPC IS SELECTED FOR EC PU = ESPI IS SELECTED FOR EC	ESPI
GPP_E19/DDPB_CTRLDATA	IPD = DO NOT DETECT PORT B PU = DETECT PORT B	DETECT PORT B
GPP_E21/DDPC_CTRLDATA	IPD = DO NOT DETECT PORT C PU = DETECT PORT C	DETECT PORT C

KBL_U_BGA1356P
6 OF 20

Memory straps pin

PCH_MEM_CFG[3:0]	MEMORY PN	QFN	Stuff
0 3210	MT52L512X32D2PF-107 WT:B	AKD5SRWDTL12	R5,R6,R7,R8
1 0001	MT52L256M32D1PF-107 WT:B	AKD5QWSLT08	R4,R5,R6,R7
2 0010	H9CCNNNB1TALAR-NUD	AKD5SRW0TW72	R3,R5,R6,R8
3 0011	H9CCNNNB8GTALAR-NUD	AKD5QW0TW38	R3,R4,R5,R6
4 0100	MT52L1G32D4PG-107	AKD5SWSLT07	R2,R5,R7,R8
5 0101	H9CCNNNCLGALAR-NUD	AKD5S0W0TW46	R2,R4,R5,R7
6 0110	NT6CL256T32CM-H1	AKD5QWSFTF00	R2,R3,R5,R8
7 0111			R2,R3,R4,R5
8 1000			
9 1001			R1,R4,R6,R7
10 1010			
11 1011			R1,R3,R4,R6
12 1100			
13 1101			R1,R2,R4,R7
14 1110			
15 1111			

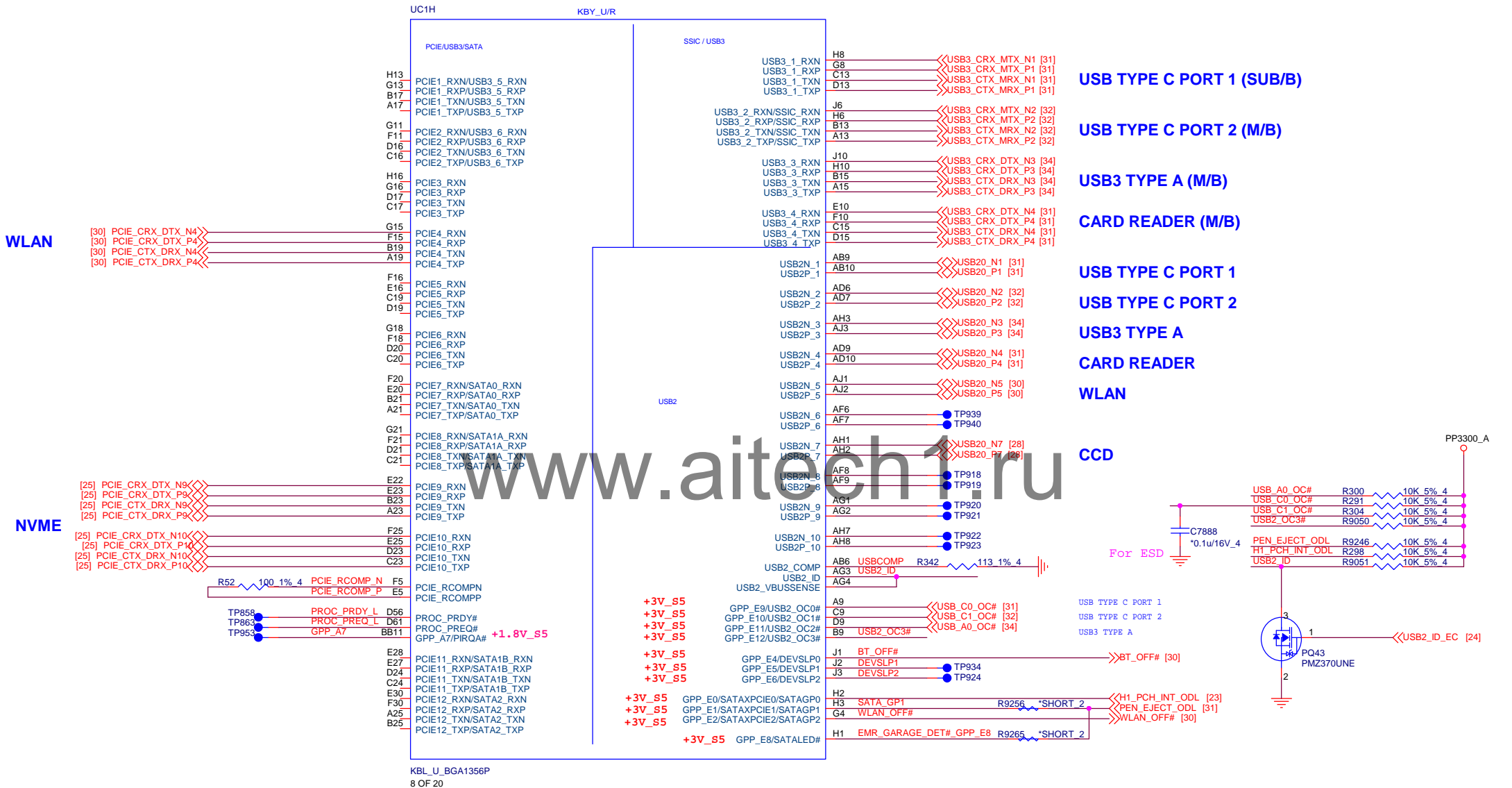


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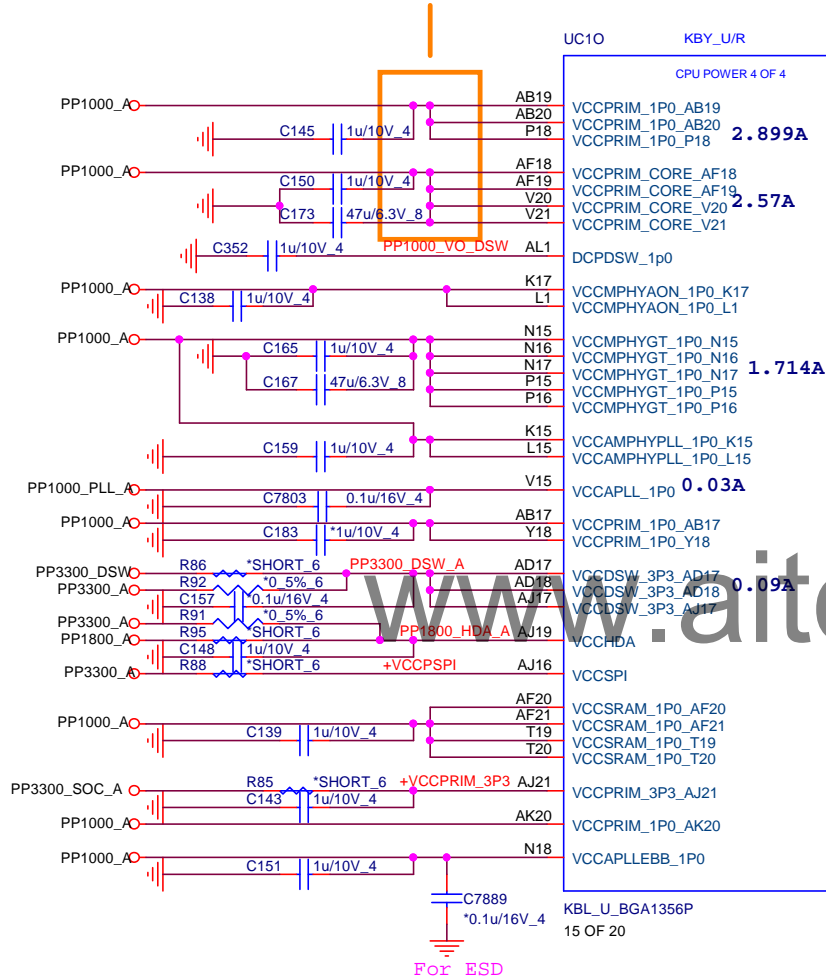
Pin Name	FUNCTION	INTENT
PCH_BUZZER	IPD = DISABLE TOP SWAP OVERRIDE PU = ENABLE TOP SWAP OVERRIDE	DISABLE
HDA_SDO/I2S_TXD0	IPD = ENABLE DESCRIPTOR SECURITY PU = DISABLE DESCRIPTOR SECURITY	ENABLE



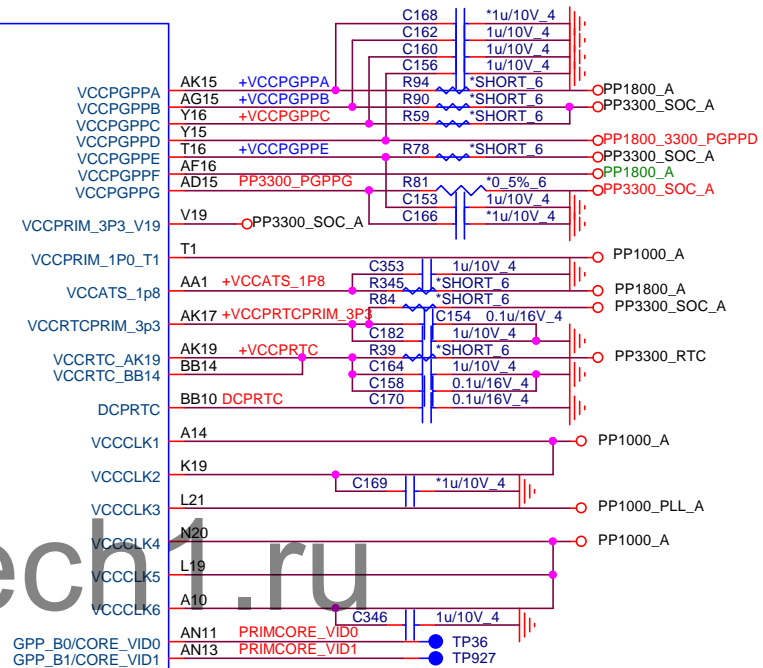
KabyLake ULT (GPU, SATA , ODD, CLK ,USB2&3)



VCCPRIM_1P0 & VCCPRIM_CORE Short

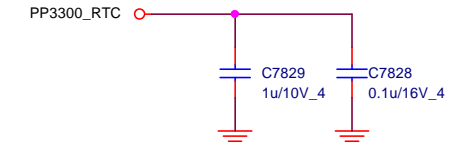


GPIO Group Power Plane



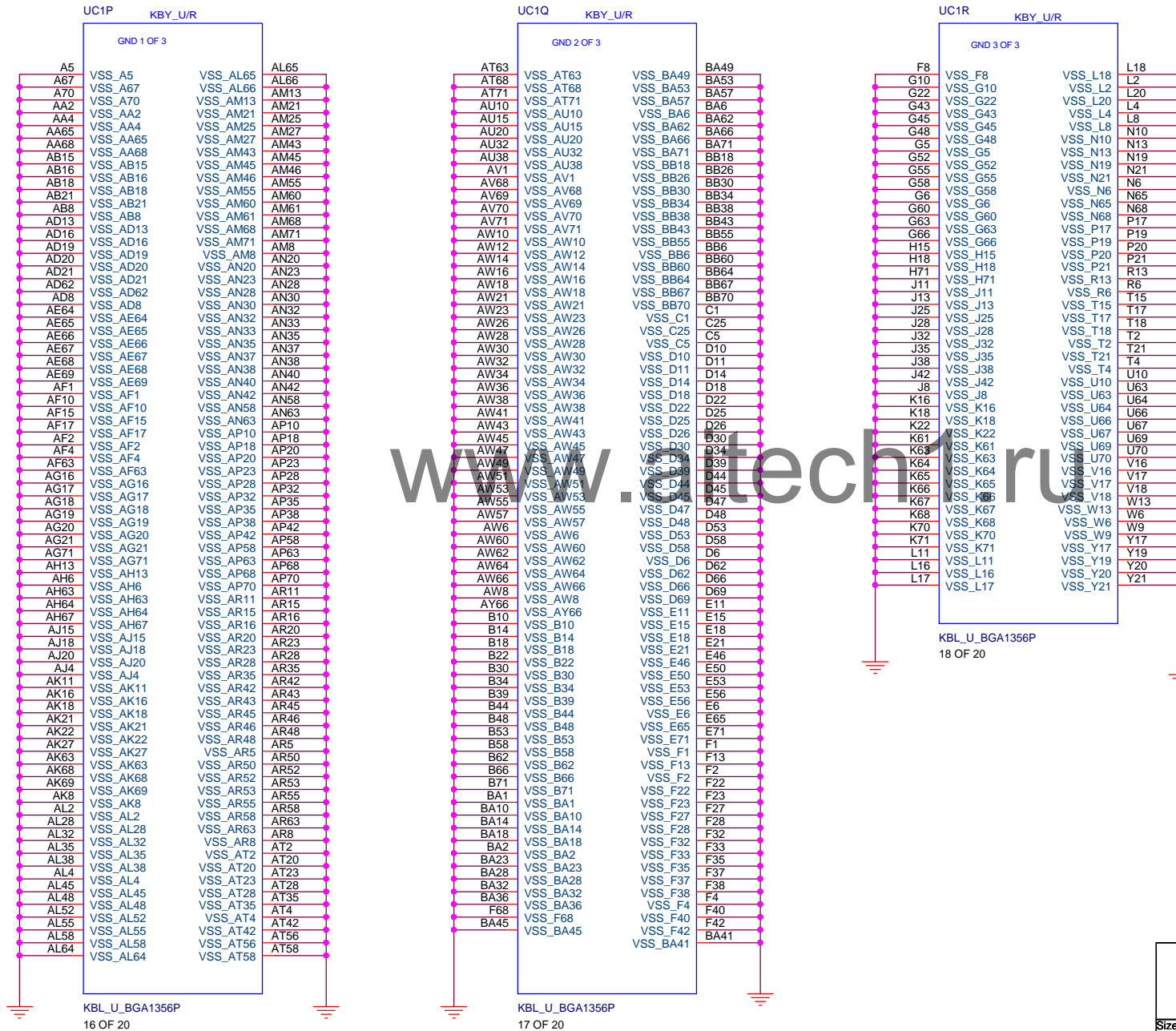
RTC Circuit

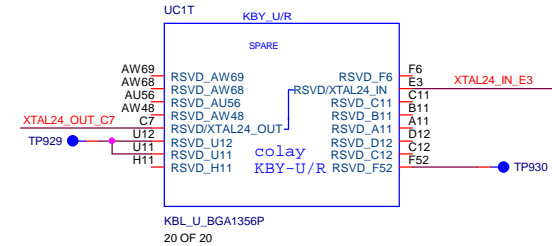
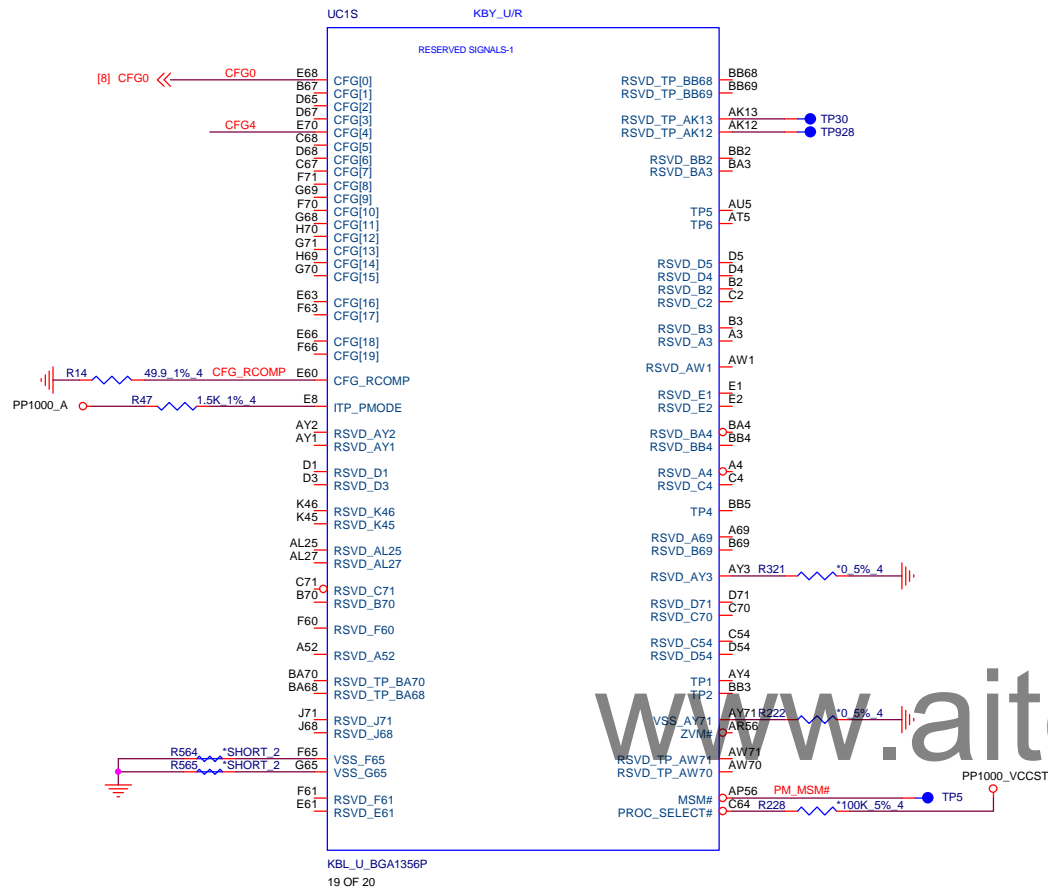
MAX 8000 mil



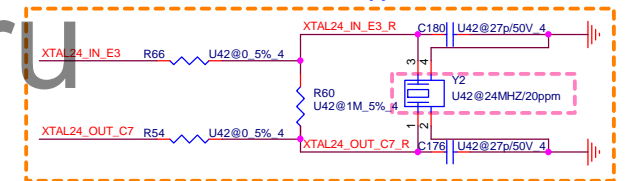
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KabyLake ULT (GND)



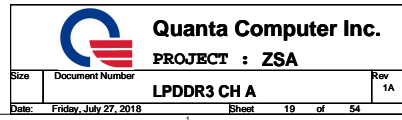


For KBL R U42
(i)Non-stuff on KBL-U

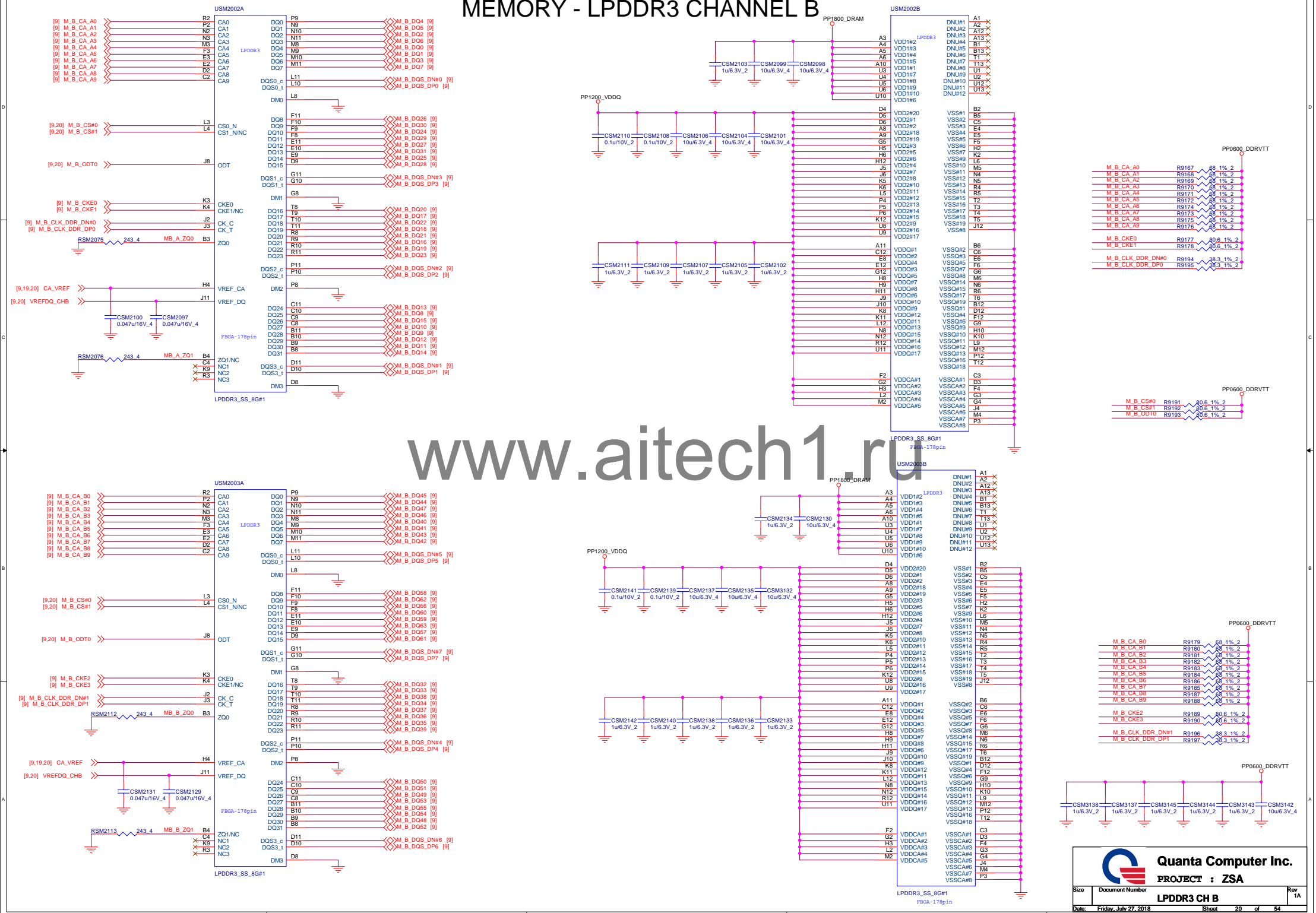


Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (iPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation(iPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) 0 = *Enabled	CFG4 R220 1K 5% 4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediately follow RESET# de-assertion (iPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		

The screenshot shows a network packet capture analysis. The packet size is 1500 bytes. The destination IP is 192.168.1.100. The packet is labeled as PP1800_DRAM.

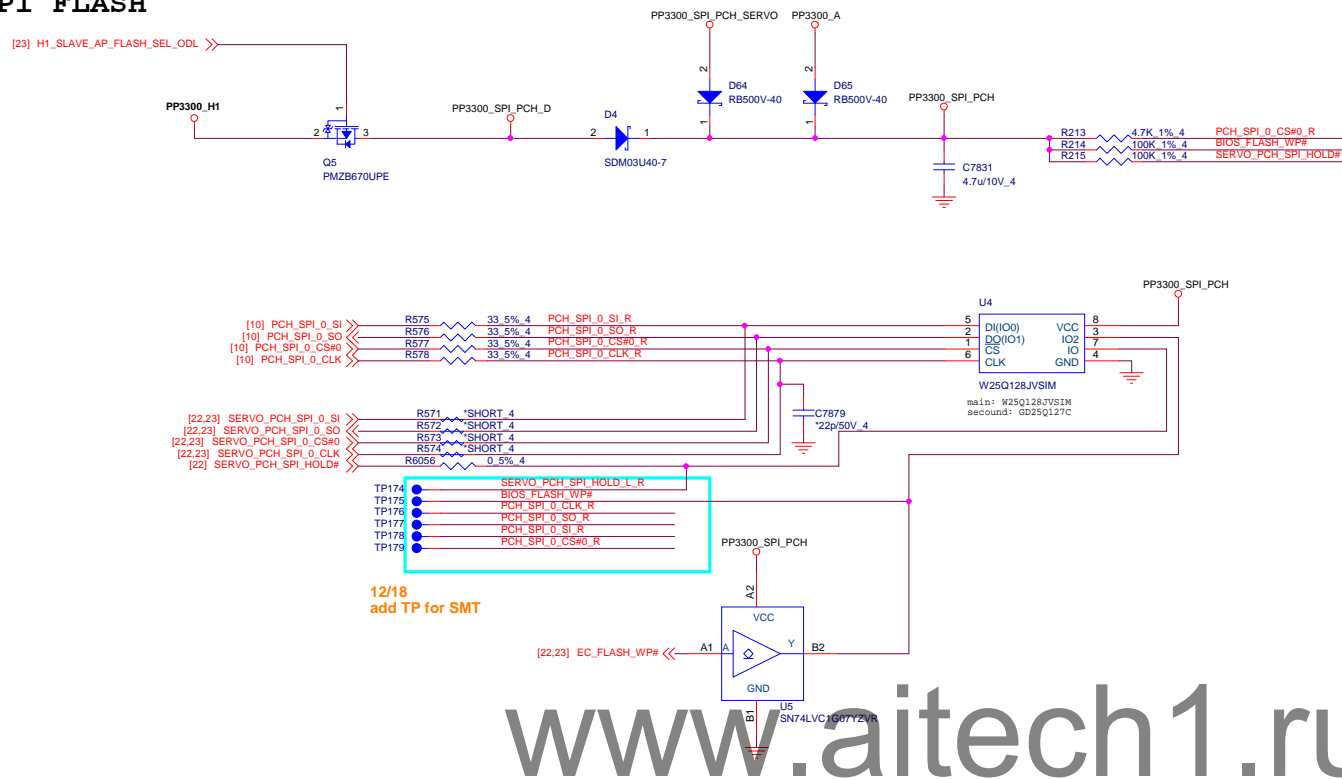


MEMORY - LPDDR3 CHANNEL B

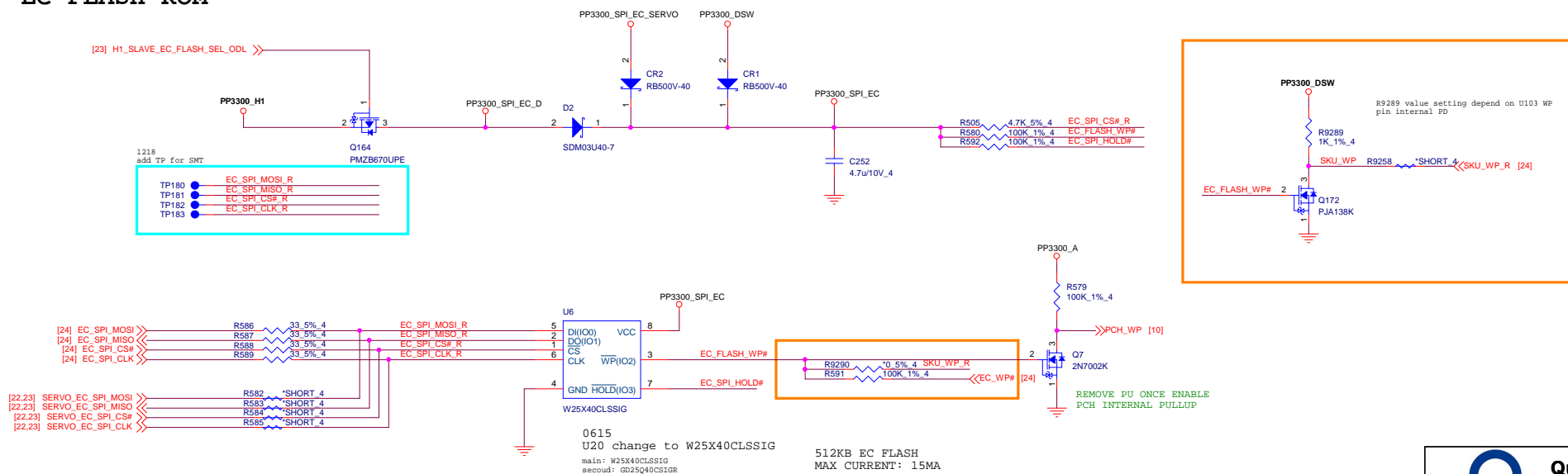


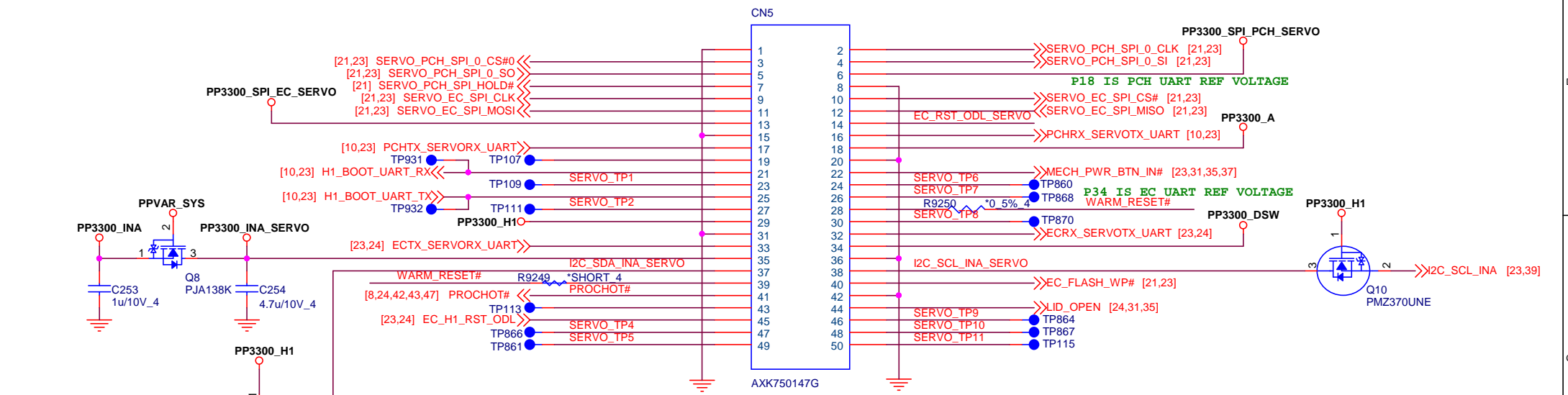
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PCH SPI FLASH

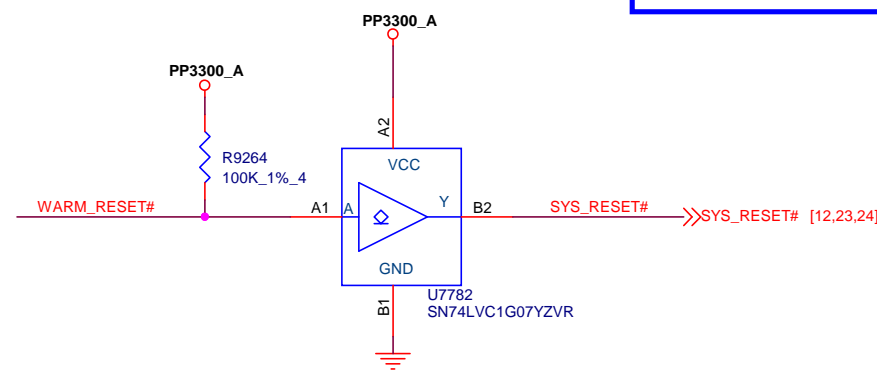


EC FLASH ROM

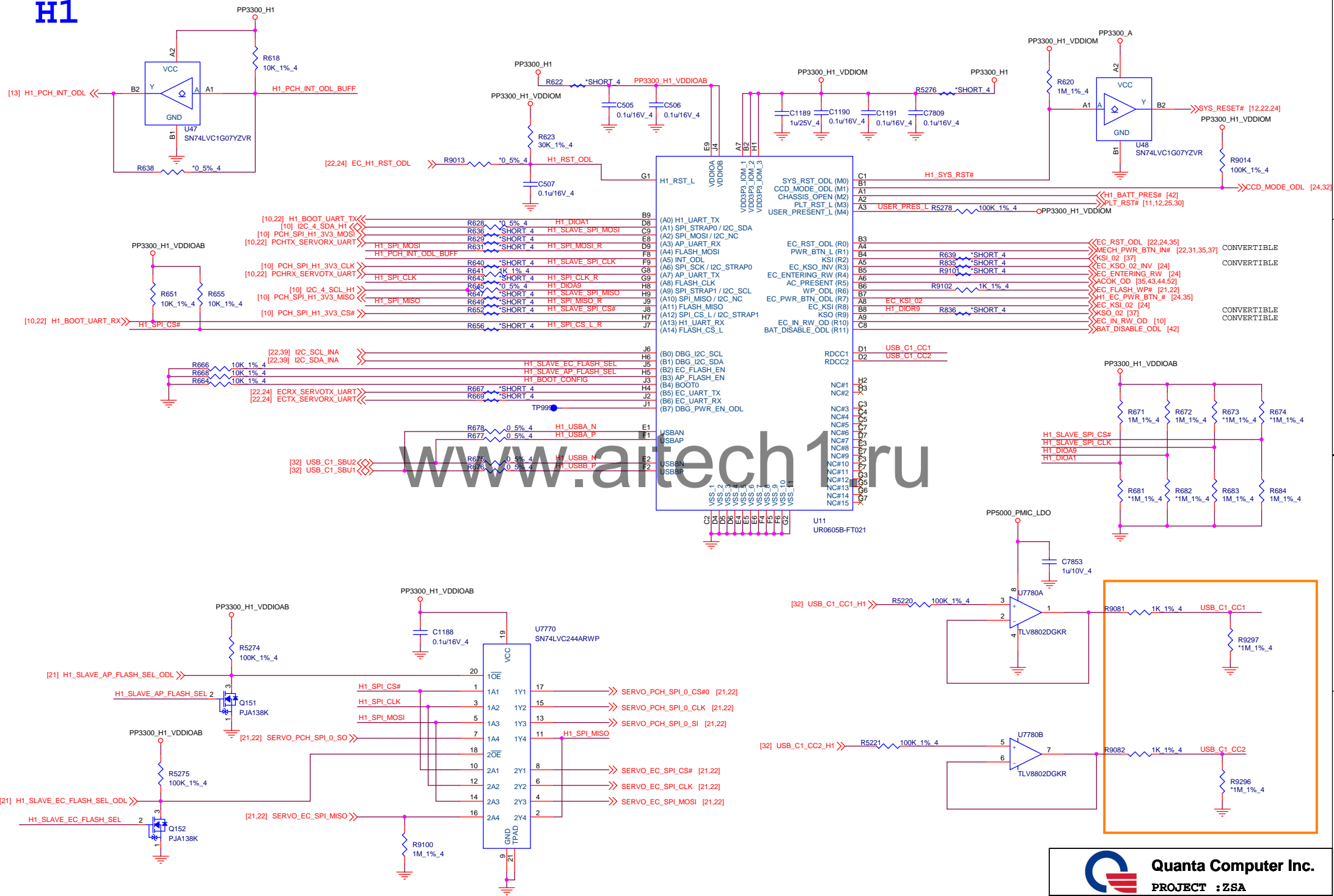


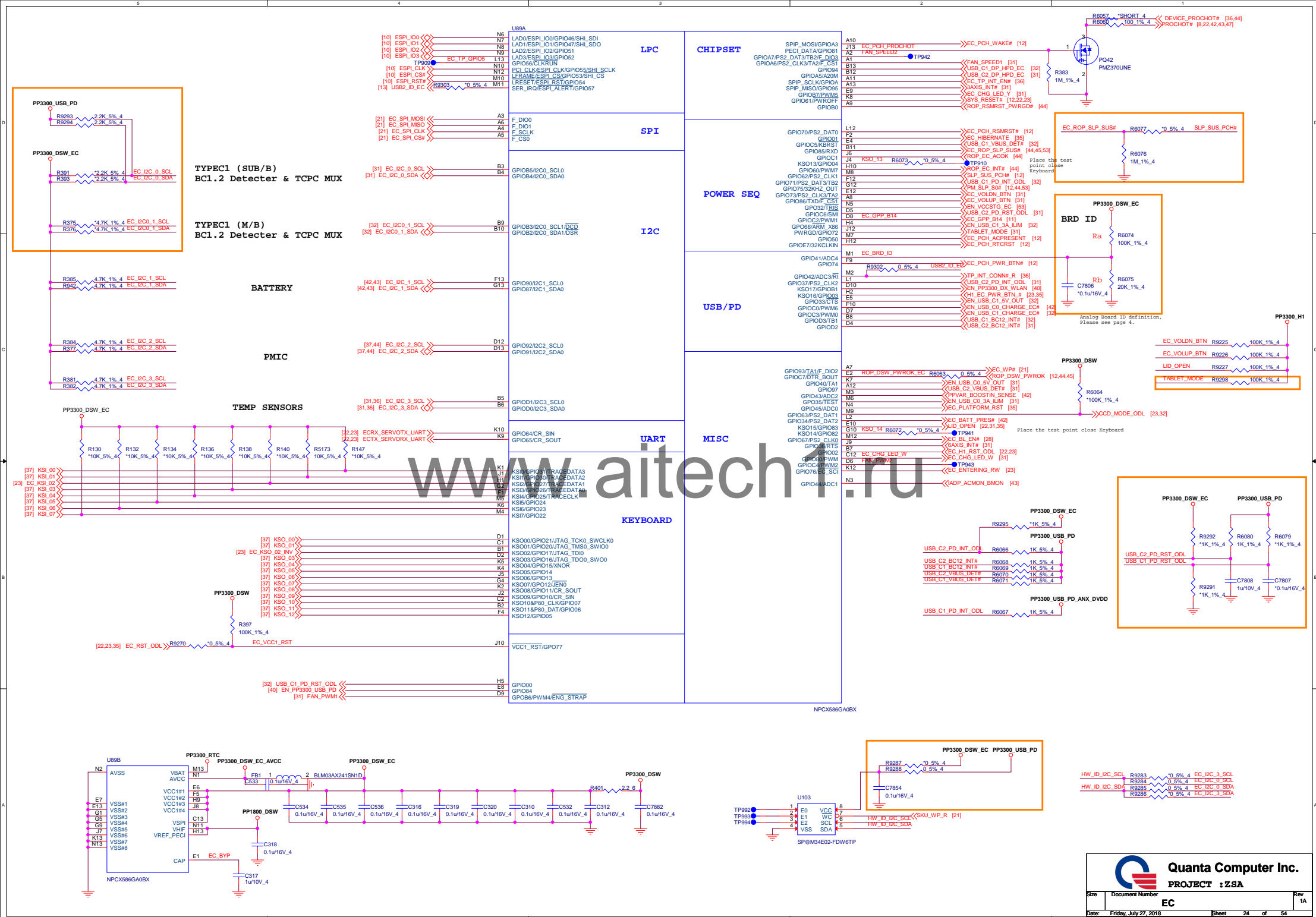


SERVO HEADER
FORCE EC TO ASSERT RSMRST# TO TRISTATE SPI BUS

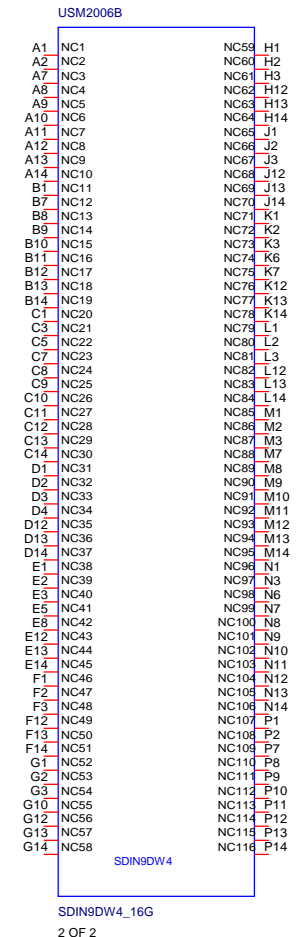
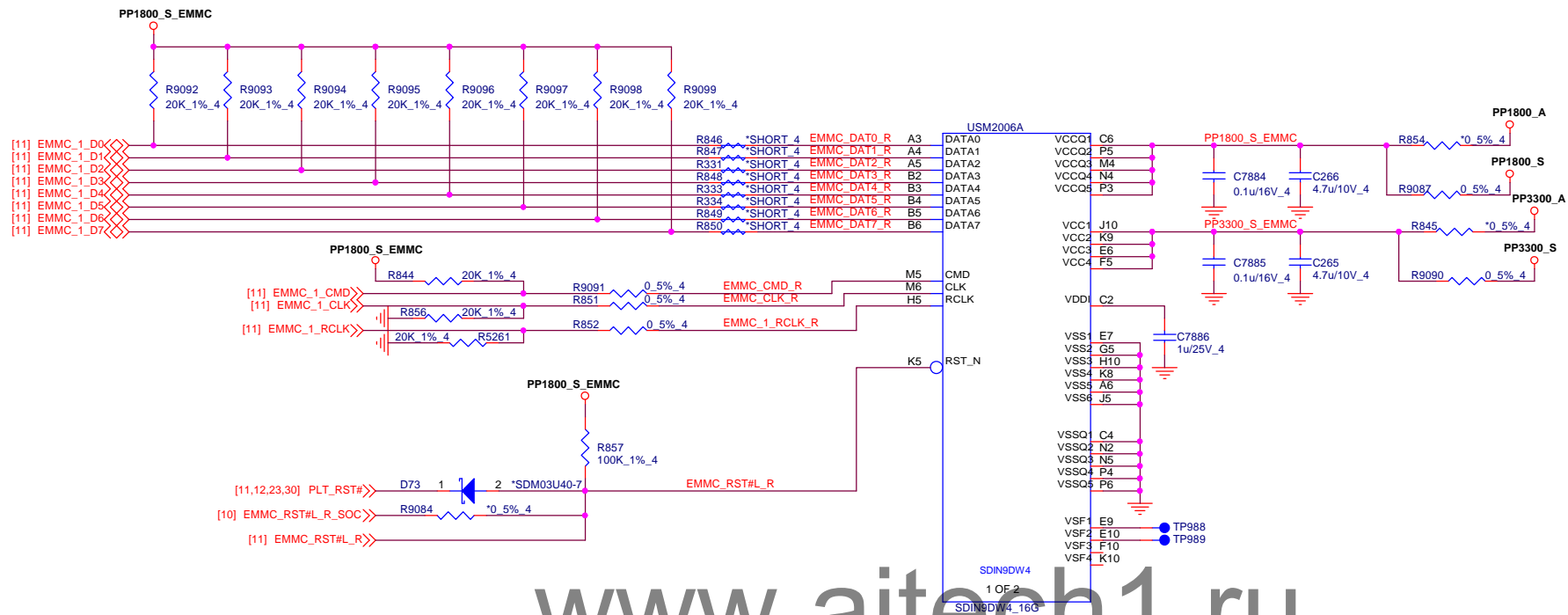


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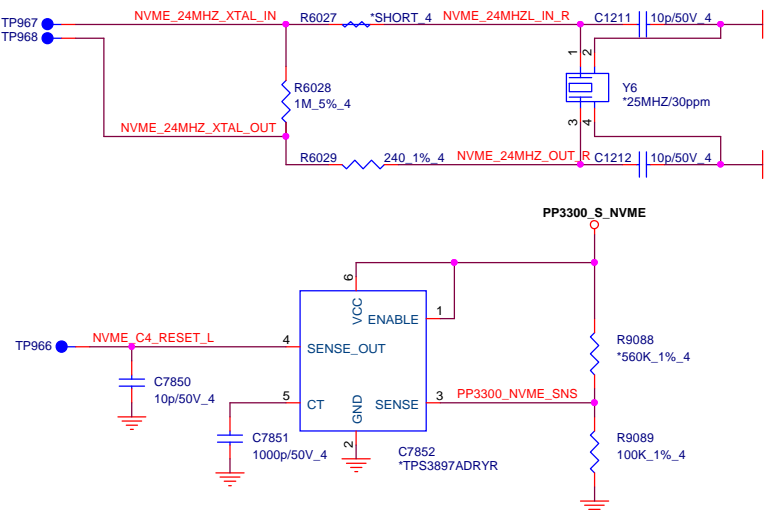
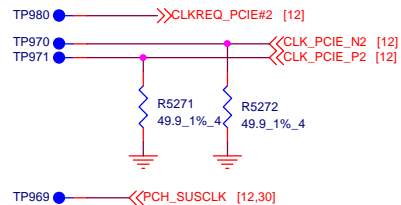
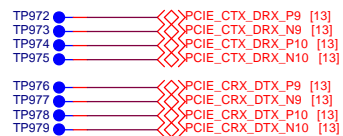
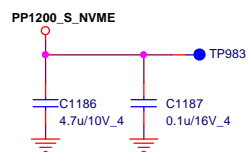
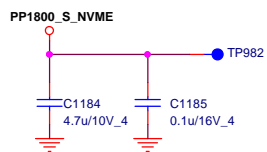




EMMC STORAGE



Reserved for NVME

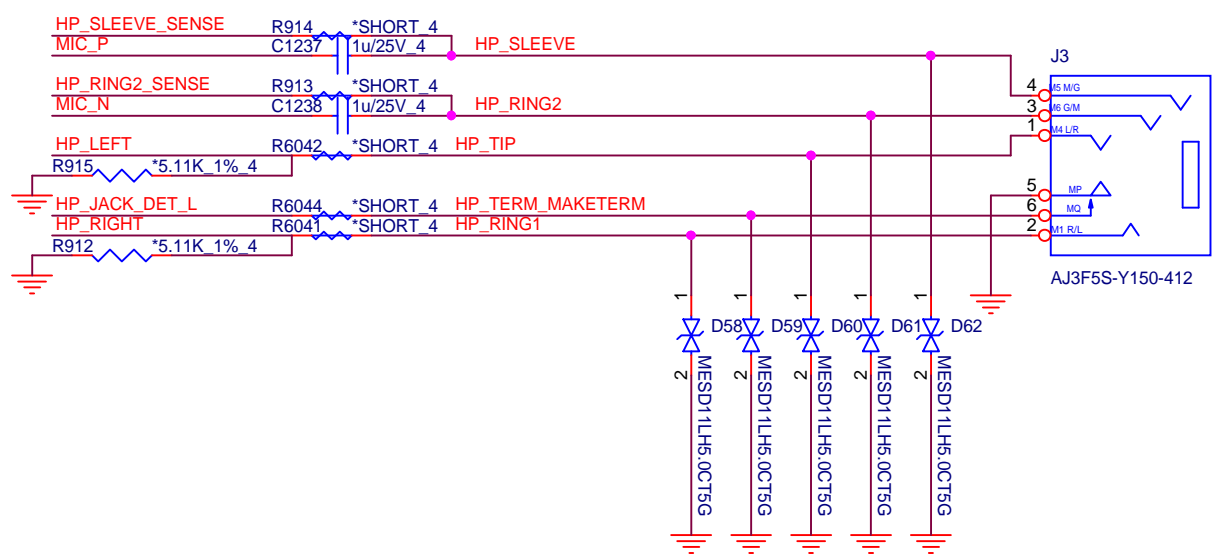
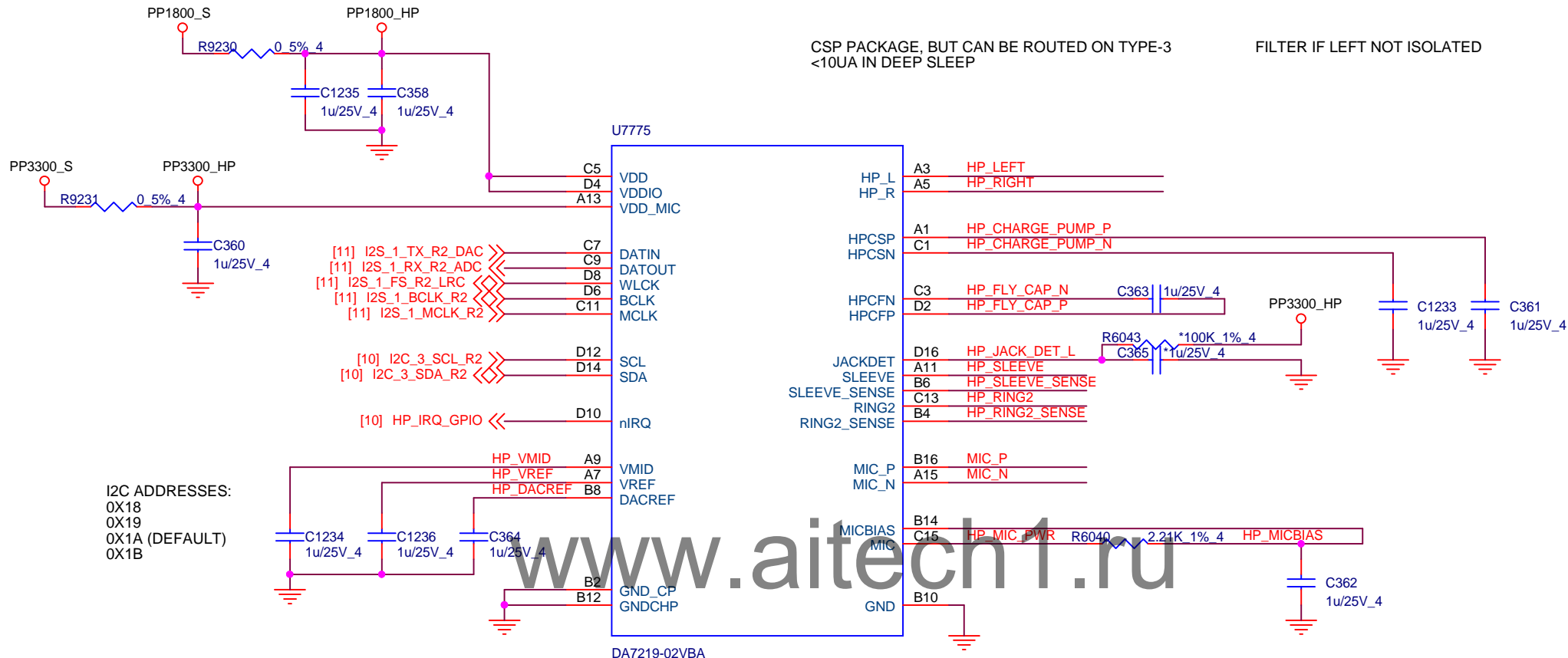



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Size Document Number EMMC/NVME Rev 1A

Date: Friday, July 27, 2018 Sheet 25 of 54

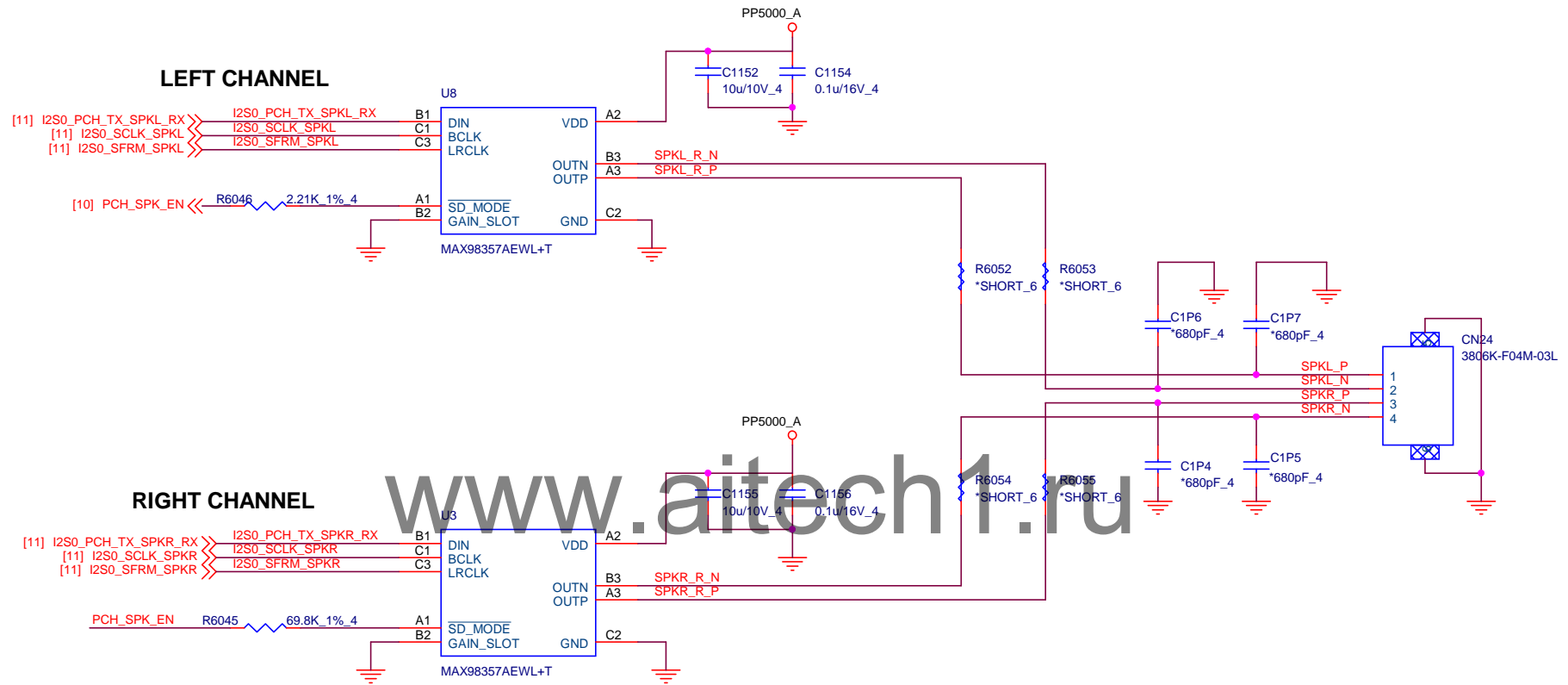




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HP AMP DA7219-02VBA

Size	Document Number	Rev 1A
Date: Friday, July 27, 2018		
Sheet 26 of 54		

MAX98357A



LRCLK POLARITY

PART NUMBER	LRCLK POLARITY (LEFT CH)
MAX98357A	LOW
MAX98357B	HIGH

BCLK POLARITY

MODE	PART NUMBER	BCLK POLARITY
I2S	MAX98357A	Rising edge
Left Justified	MAX98357B	Rising edge
TDM	MAX98357A	Rising edge
	MAX98357B	Falling edge

GAIN TABLE

GAIN_SLOT	GAIN(dB)
PL 100K TO GND	15
PL TO GND	12
FLOATING	9
PU TO VDD	6
PU 100K TO VDD	3

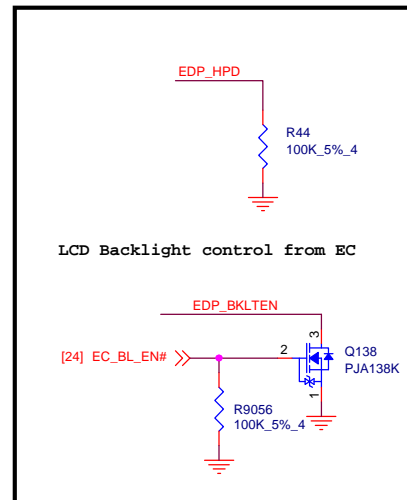
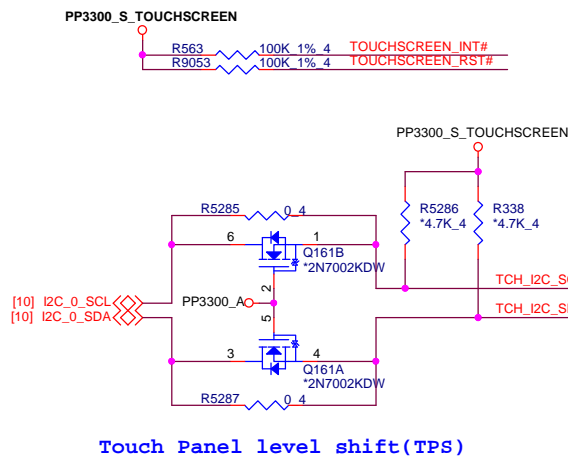
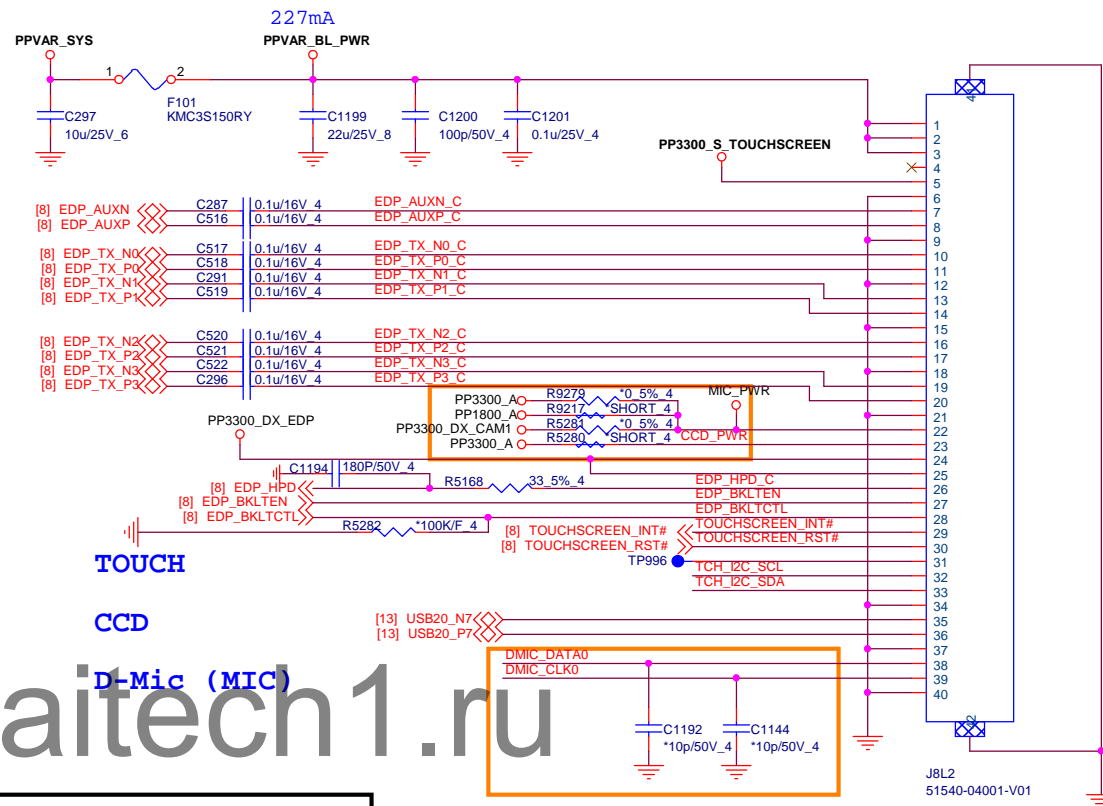
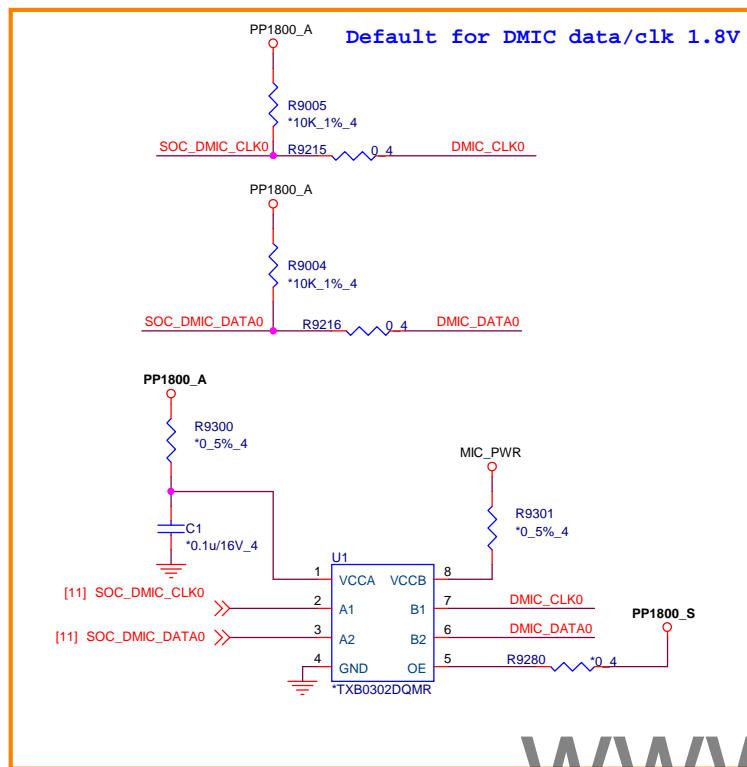


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AUDIO - SPEAKER AMPS

Size	Document Number	Rev 1A
Date:	Friday, July 27, 2018	Sheet 27 of 54



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PROJECT : ZSA

Size	Document Number	Rev
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Date:	Friday, July 27, 2018	Sheet 28 of 54

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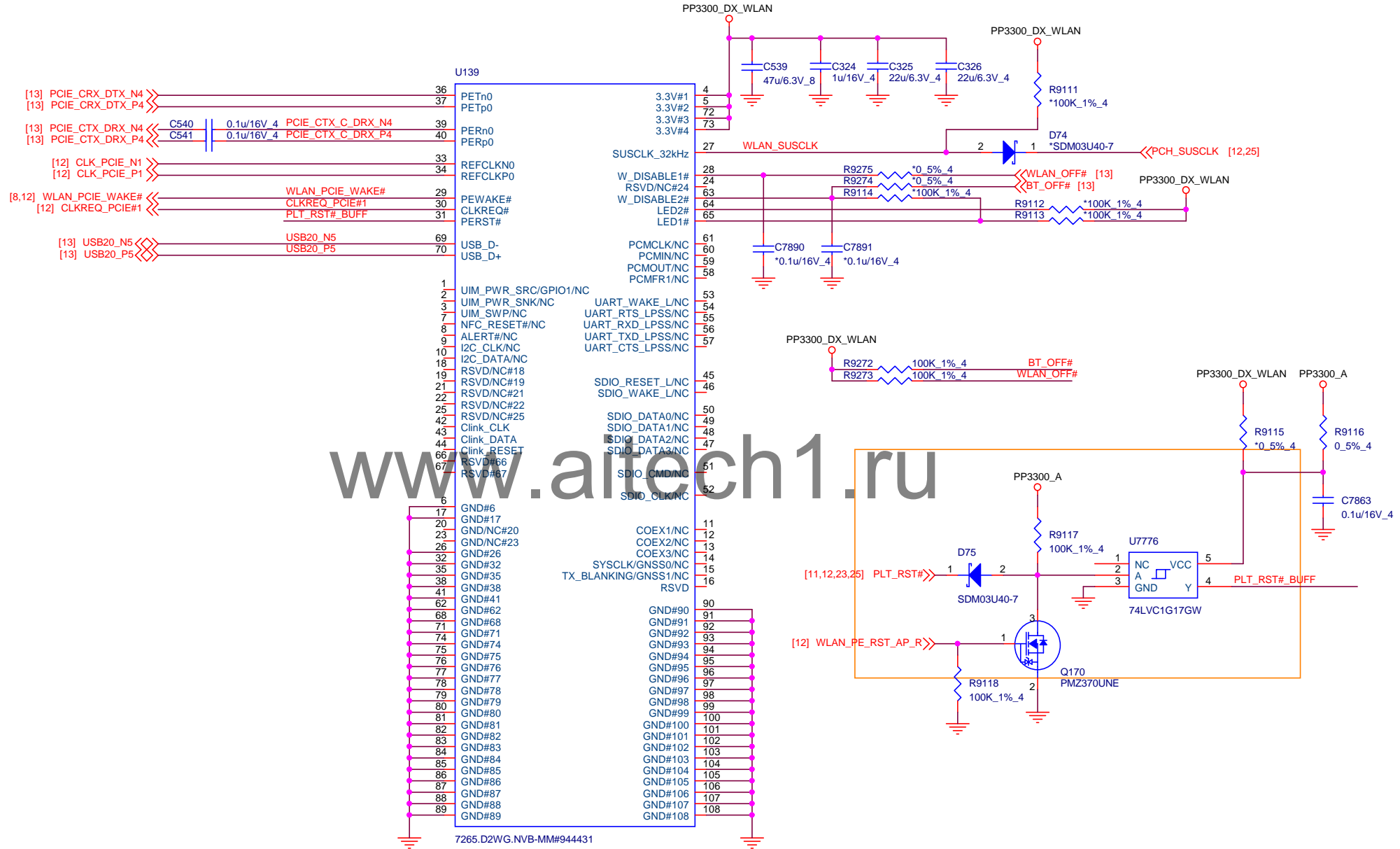


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Size	Document Number	Rev
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Date:	Friday, July 27, 2018	Sheet 29 of 54

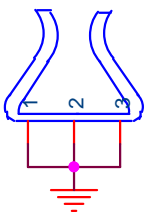
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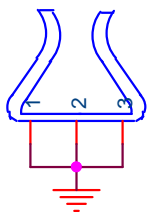
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CLIP

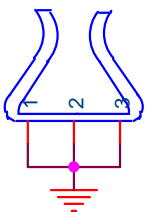
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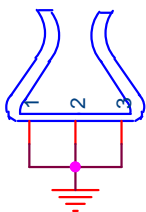
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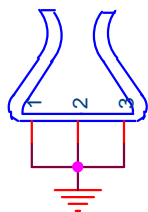
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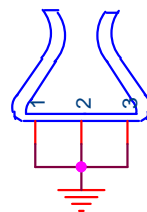
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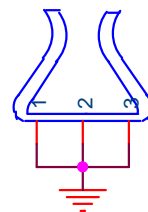
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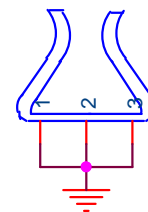
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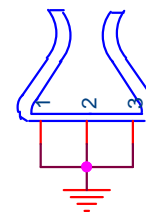
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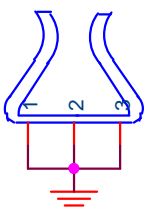
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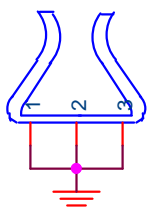
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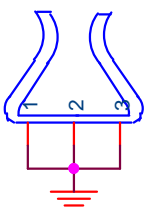
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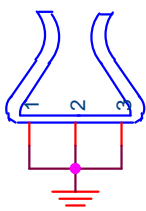
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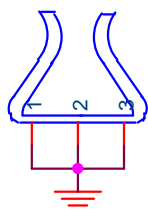
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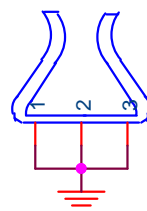
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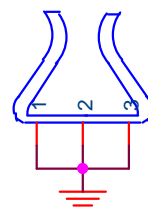
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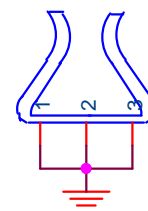
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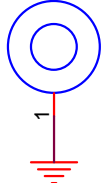
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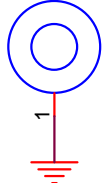
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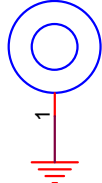
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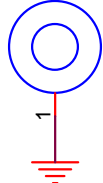
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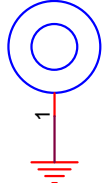
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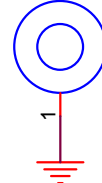
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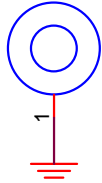
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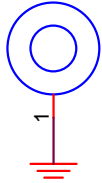
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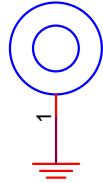
HOLE15
*H-TC236BC197D150P2



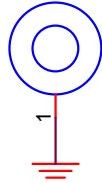
HOLE18
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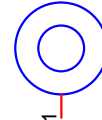
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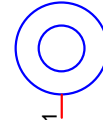
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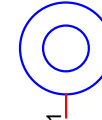
HOLE8
*H-C98D98N



HOLE16
*H-C177D177N



HOLE17
*H-O110X98D110X98N



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PROJECT :

PCB, Screw, CLIP

Size

Document Number

Rev
1A

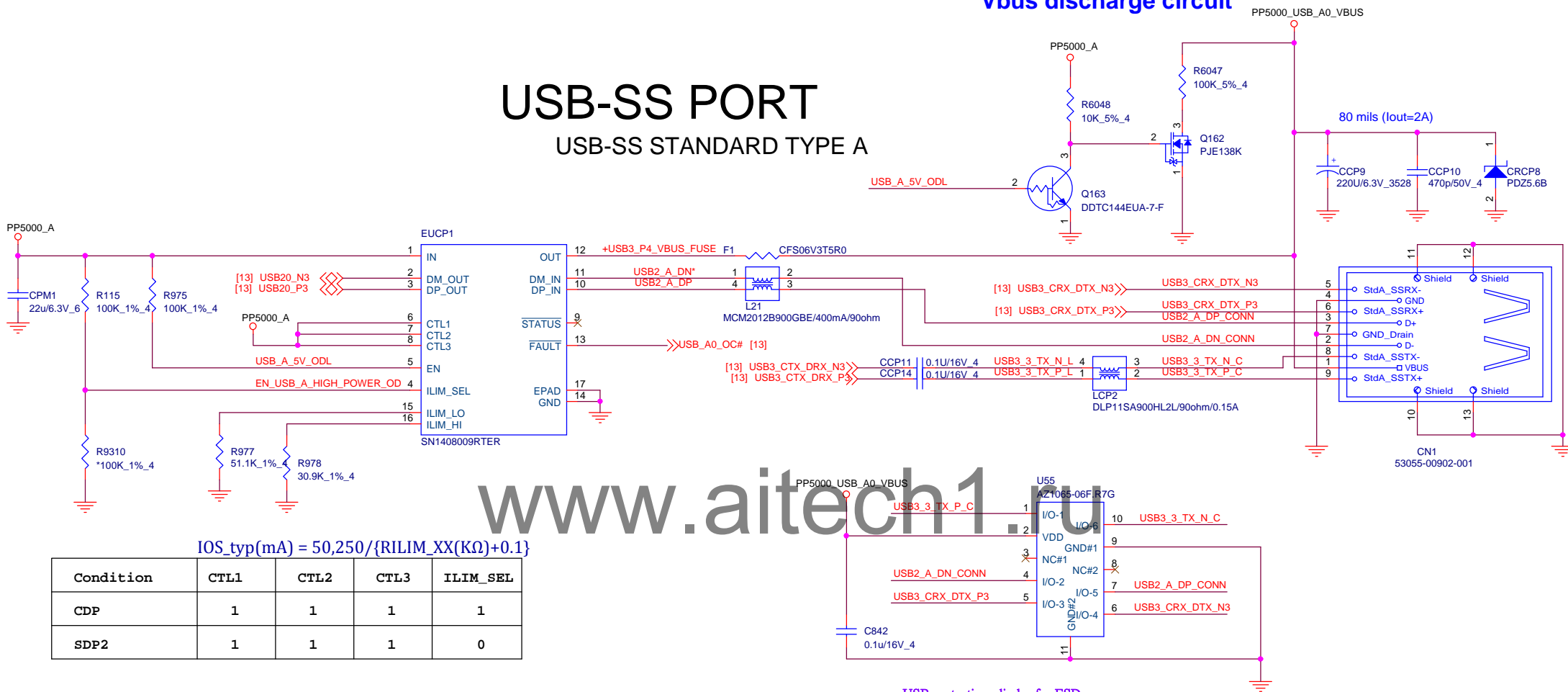
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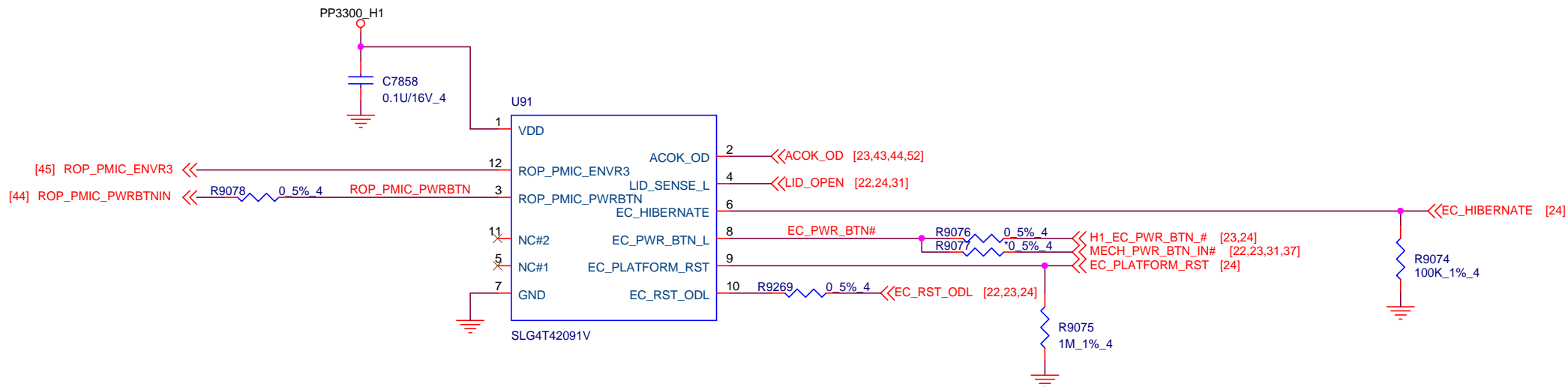
Sheet 33 of 54

USB-SS PORT

USB-SS STANDARD TYPE A

Vbus discharge circuit

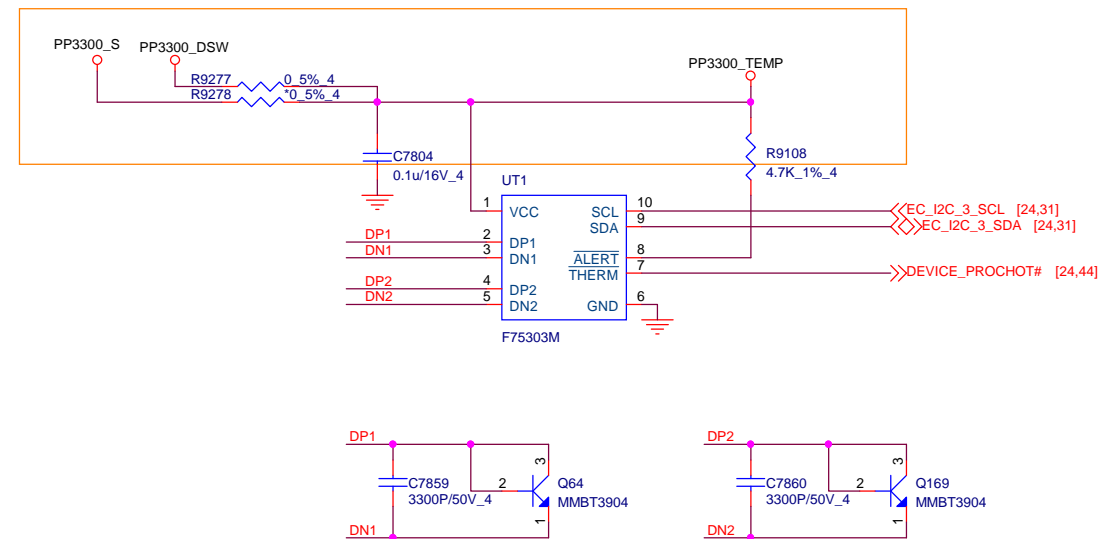




Pin Configuration

Pin#	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	1M ohm pullup
2	ACOK_OD	Digital Input	Digital Input without Schmitt trigger	1M ohm pullup
3	ROP_PMIC_PWRBTN	Digital Output	Open Drain NMOS 1X	floating
4	LID_SENSE_L	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
5	NC	--	Keep Floating or Connect to GND	--
6	EC_HIBERNATE	Digital Input	Digital Input without Schmitt trigger	floating
7	GND	GND	Ground	--
8	EC_PWR_BTN_L	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
9	EC_PLATFORM_RST	Digital Input	Digital Input without Schmitt trigger	floating
10	EC_RST_ODL	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
11	NC	--	Keep Floating or Connect to GND	--
12	ROP_PMIC_ENVR3	Digital Output	Open Drain NMOS 1X	floating

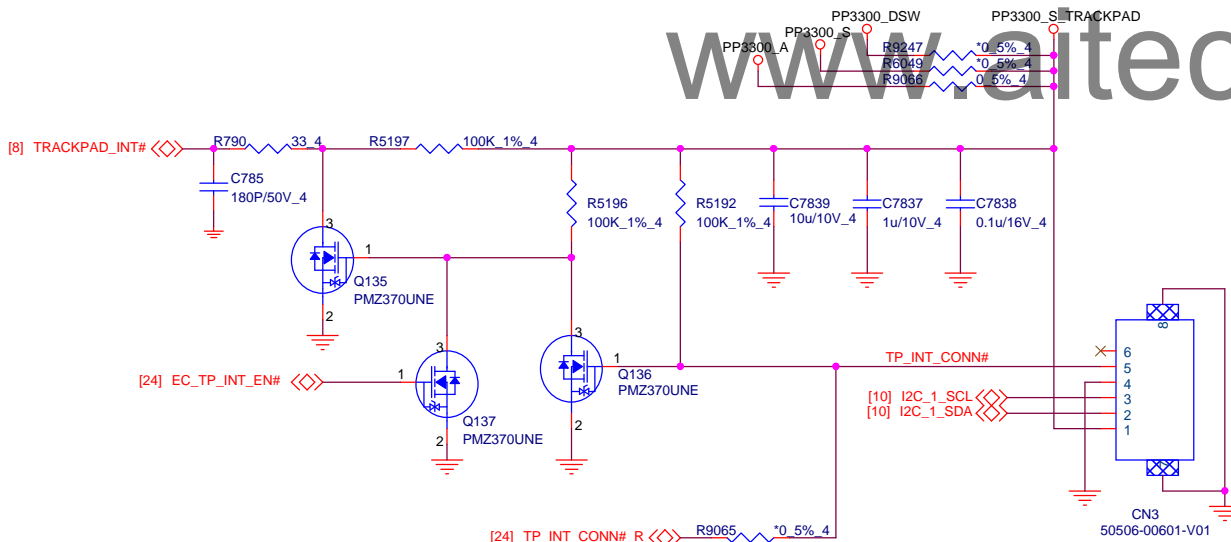
TEMP SENSORS



TRACKPAD CONNECTOR

Due to 3906 transistors is not common component in Quanta.
Could we replace 3906 transistors by 3904 transistors?
These two parts are substitute component in datasheet.

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ELAN CLICK PAD
P/N: SA461D-1008, Rev.1.0

4.4 Pin Assignment

Pin Assignment and Description			
Pin #	Signal	I/O	Description
1	NC		NC
2	/SINT	O	Slave interrupt Indicates touchpad likes to send data to system (host)
3	GND	GND	Ground
4	I ² C_CLK	I/O	I ² C clock I _{Drive} or I _{Sink} : 8 mA max.
5	I ² C_DATA	I/O	I ² C data. I _{Drive} or I _{Sink} : 8 mA max.
6	VCC_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.



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PROJECT : ZSA

Size Document Number Rev 1A

Trackpad/Thermal

Date: Friday, July 27, 2018 Sheet 36 of 54

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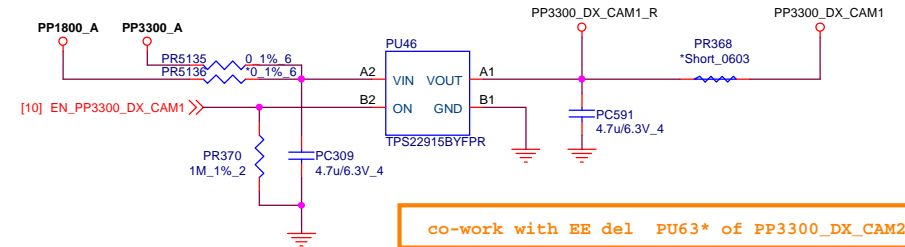
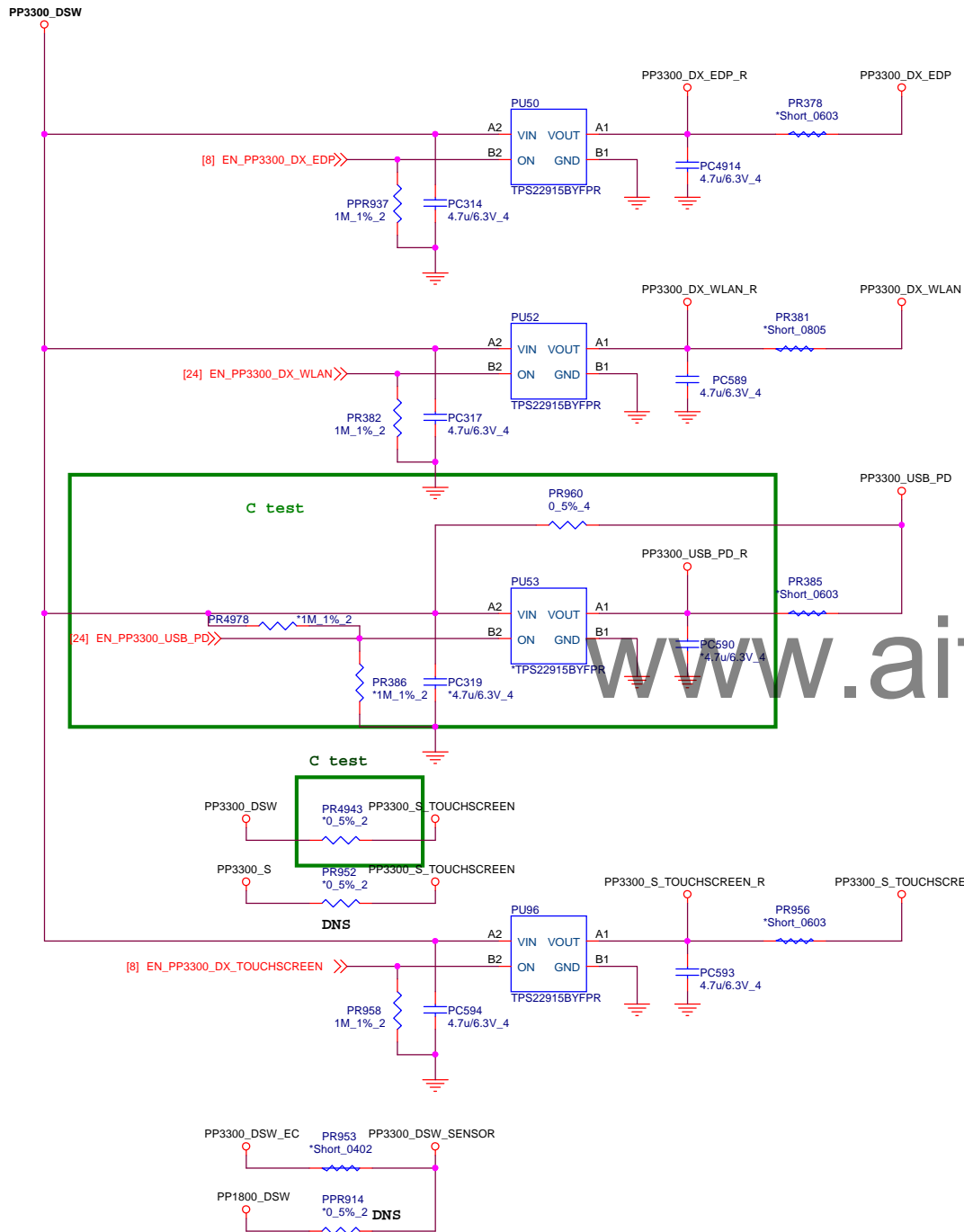


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PROJECT : ZSA

Size	Document Number	Rev
	BLANK	1A
Date:	Friday, July 27, 2018	Sheet 38 of 54

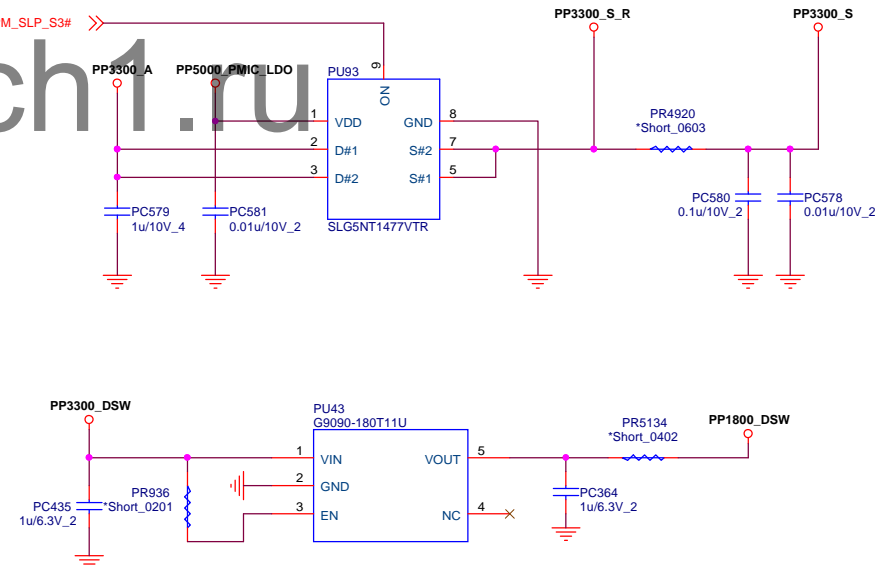
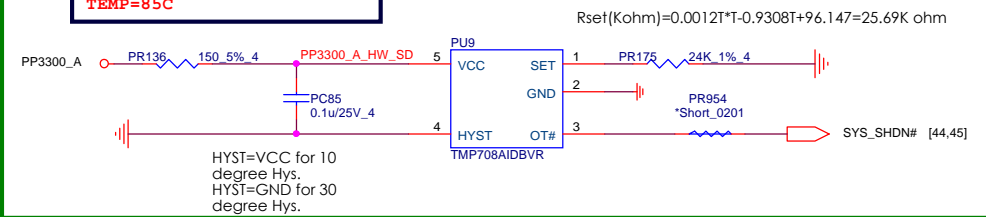
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Thermal protection

For thermal protect point
Note placement position
TEMP=85C

C test



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PROJECT :

LOAD SWITCHES

Size	Document Number	Rev
1A		

Date: Friday, July 27, 2018

Sheet 40 of 54

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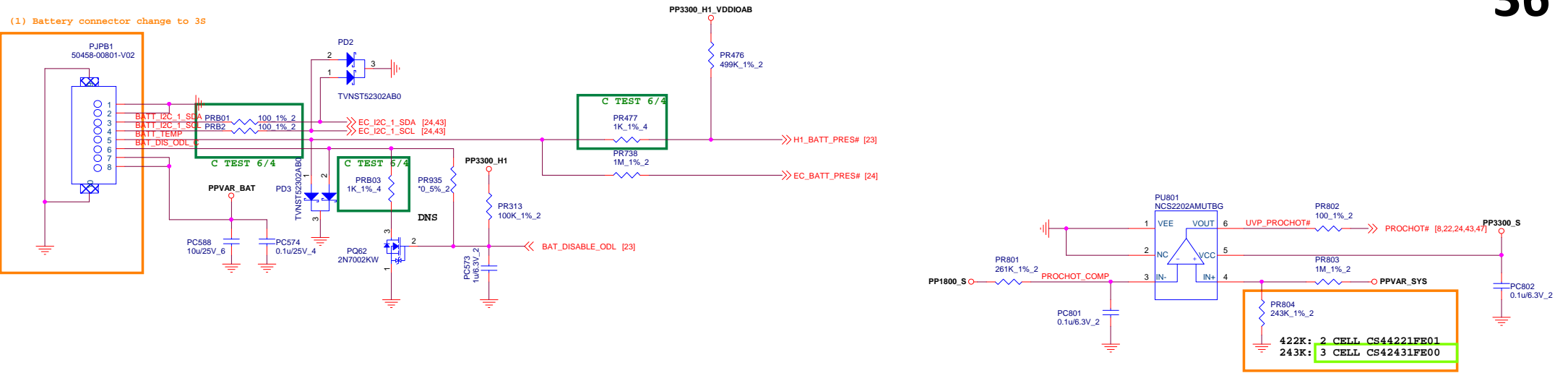


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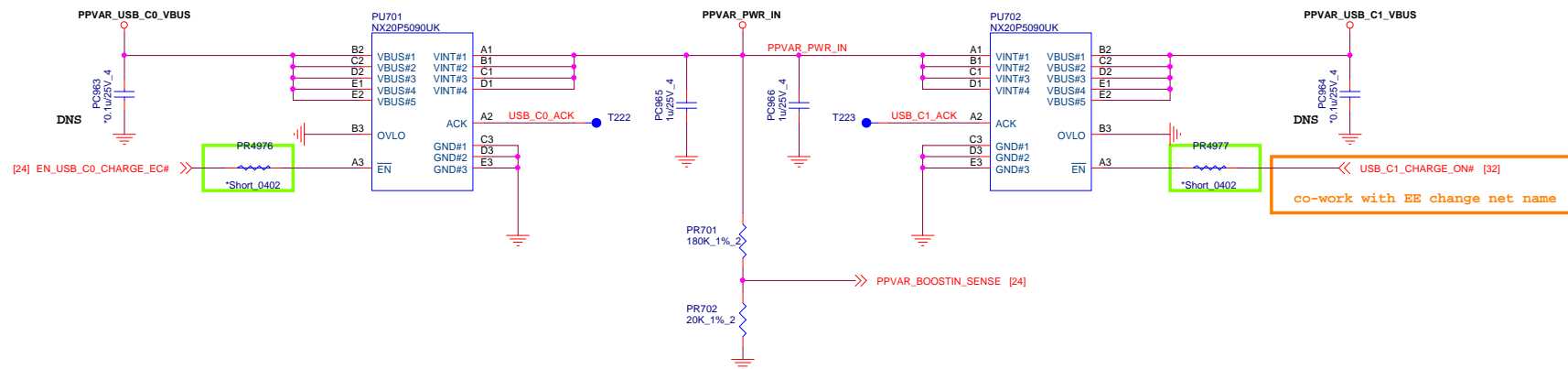
PROJECT : ZSA

Size	Document Number	Rev
	BLANK	1A
Date:	Friday, July 27, 2018	Sheet 41 of 35

(1) Battery connector change to 3S



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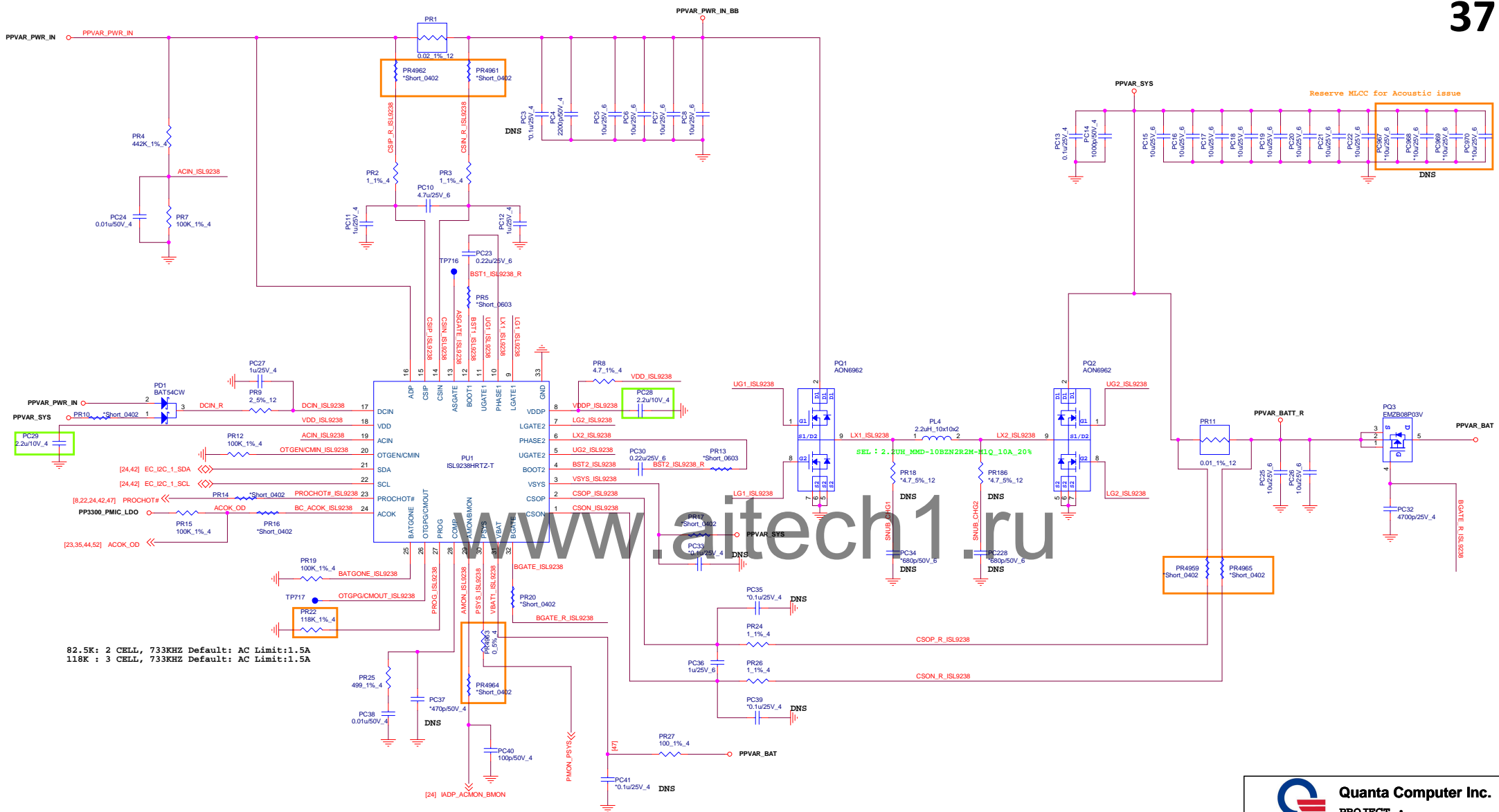


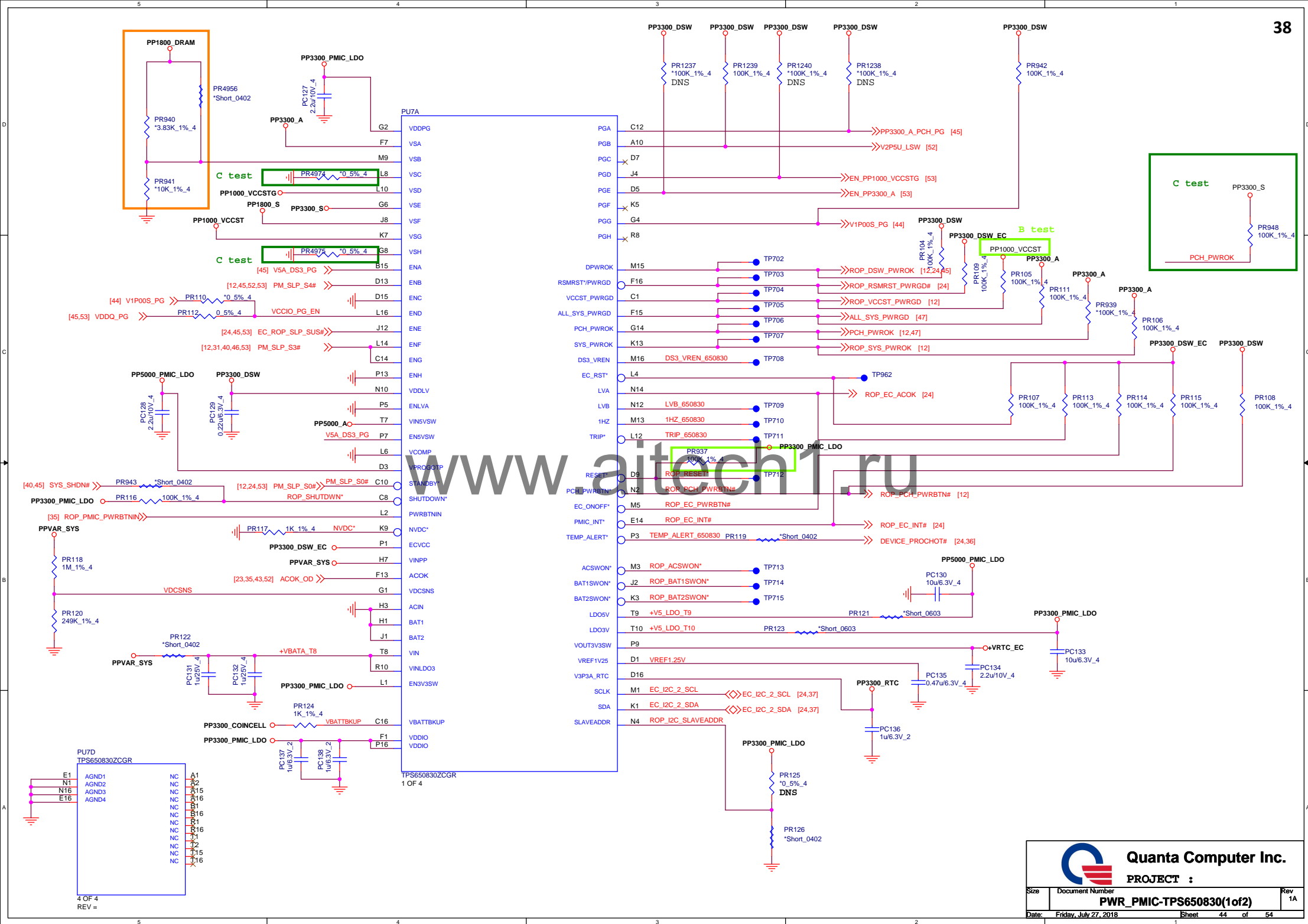
Quanta Computer Inc.

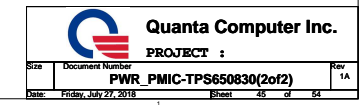
PROJECT :

PWR_AC/DC CONN/OTP

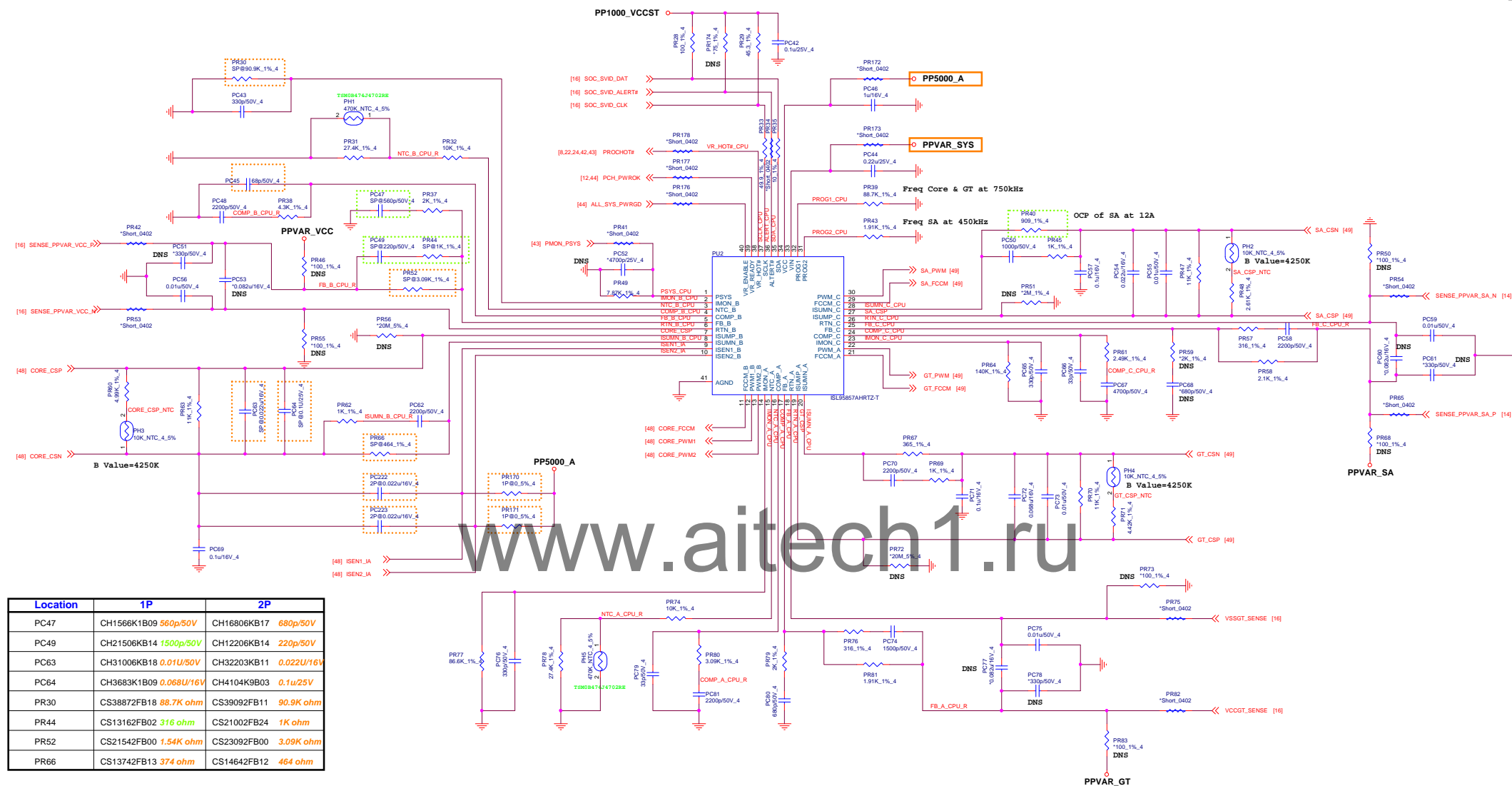
Size	Document Number	Rev
		1A
Date:	Friday, July 27, 2018	Sheet 32 of 44

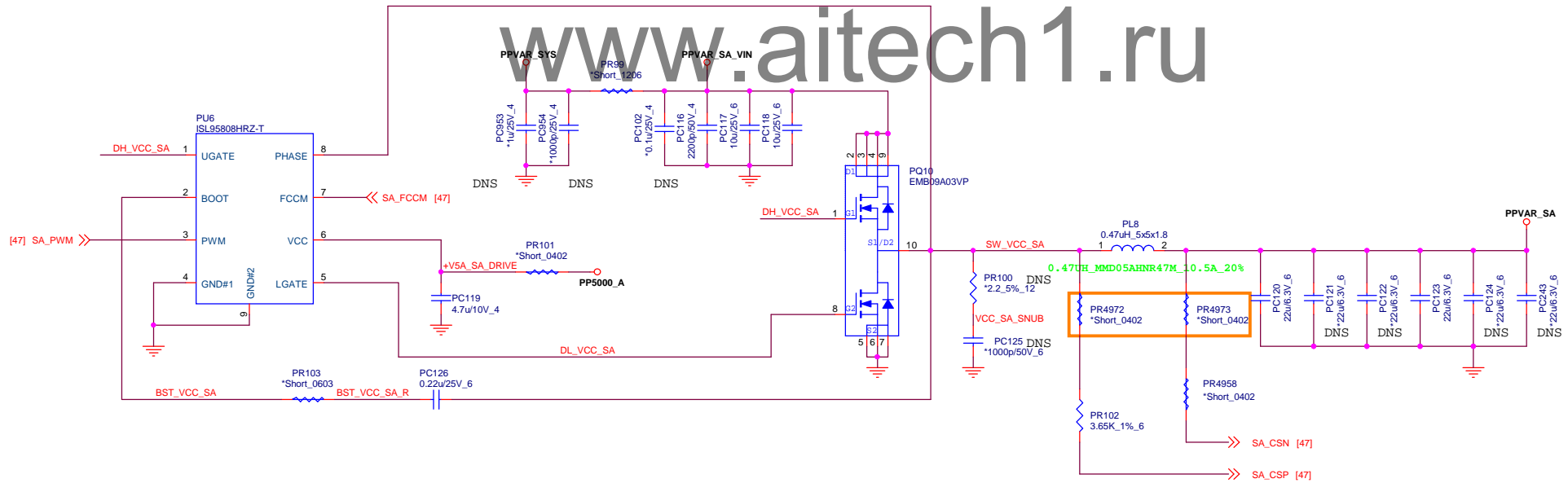
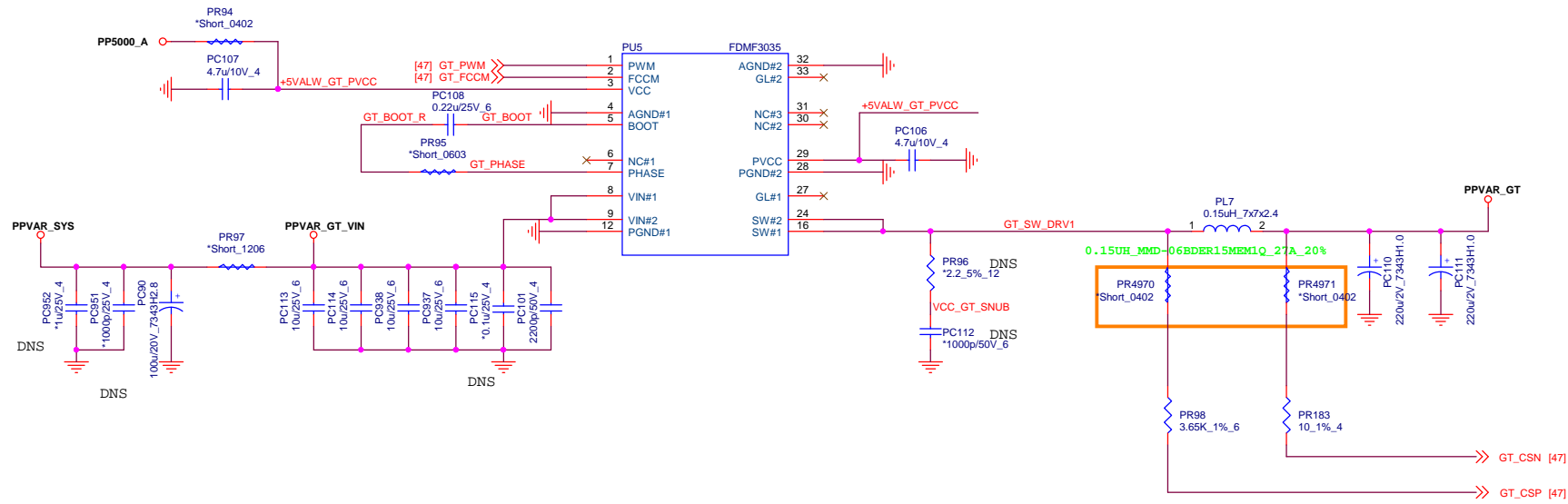






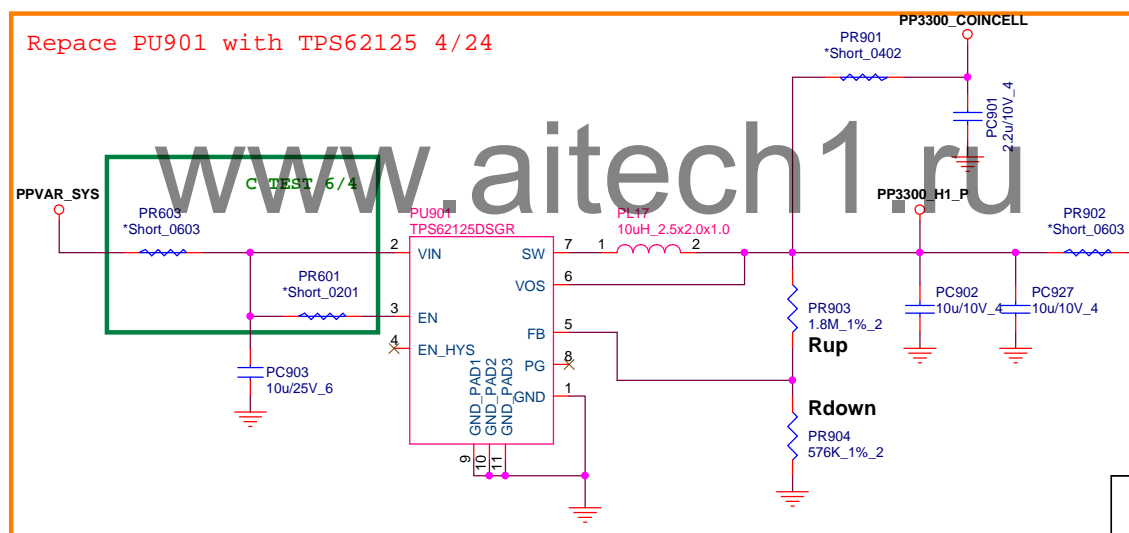
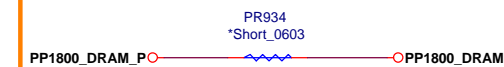
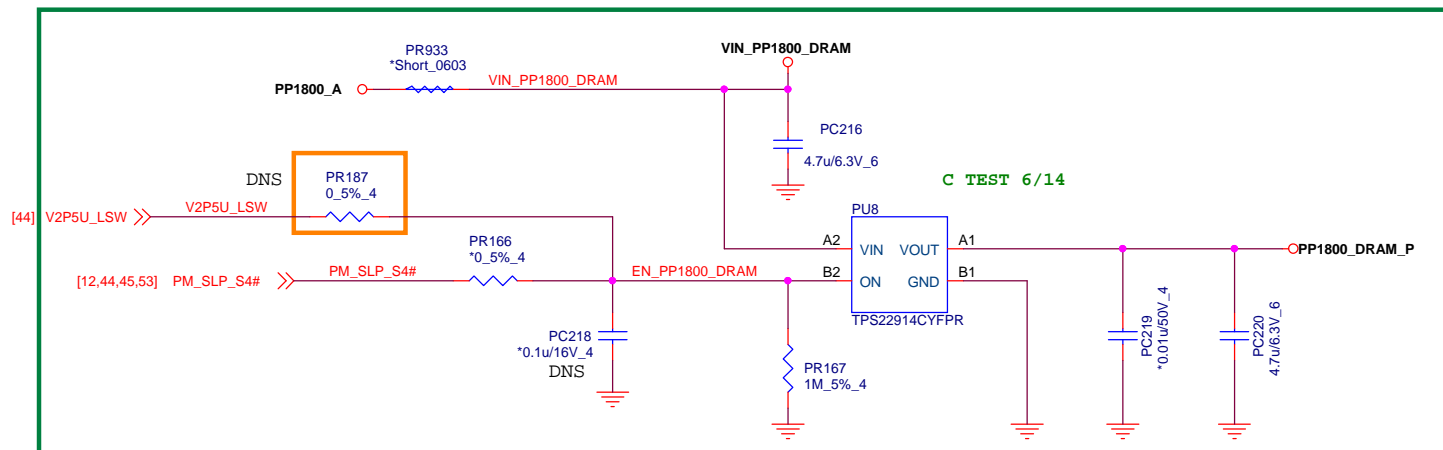






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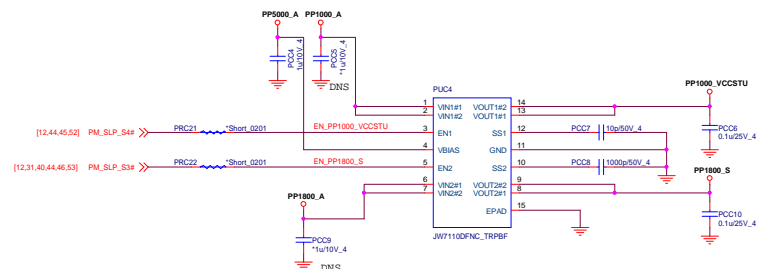
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PROJECT :

PWR_ROP

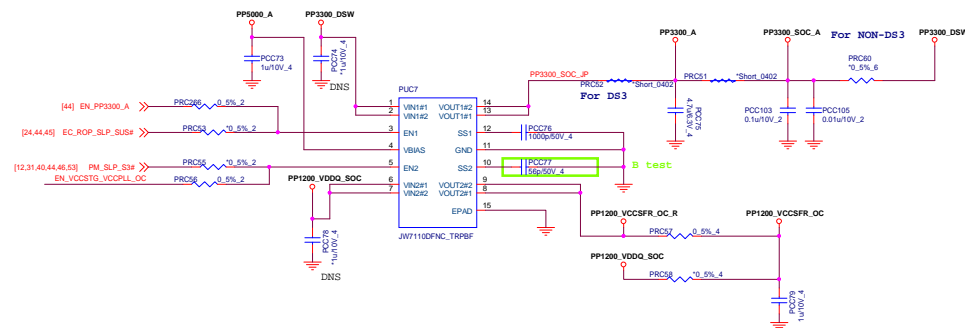
Size	Document Number	Rev
		1A
Date:	Friday, July 27, 2018	Sheet 52 of 54

PP1000_A TO PP1000_VCCSTU

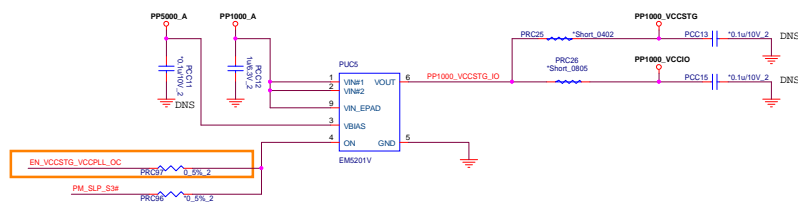


PP1800_A TO PP1800_S

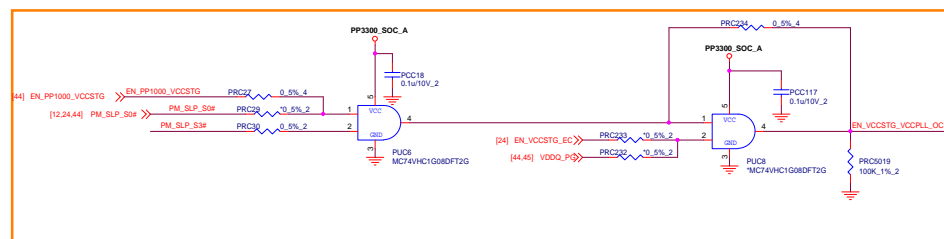
PP3300_A TO PP3300_SOC_A





PP1000_A TO PP1000_STG / PP1000_VCCIO



co-work with EE del PUC8



Model		Version	CHANGE LIST			
		1A	1. First release			
		1B	1. page 42: Change PJPB1 Battery connector for 3S Battery 2. page 43: PR22 from 82.5K change to 118K for 3S battery 3. page 44: Vendor suggest add PR4974 and PR4975 Connect VSC and VSH unused pins to GND better than let them floating 4. page 44: Add PR4956 for PP1000DRAM 5. page 45: Add PR4951,PR4952,PR4953,PR4954 for LPDDR3_DRAM 6. page 47: Change net to correct form PP1000_ST change to PP1000_VCCST 7. page 47: Change net to correct PU2 PIN 33 VIN net to PPVAR_SY5_PIN34 VCC net to PP5000_A 8. page 52: PR158 change to 12.7K for LPDDR3_DRAM 9. page 52: Net form PP2500_DRAM change to PP1800_DRAM, for LPDDR3_DRAM 10. MAG Inductor form xsl change to xsq (L&Q inner code, Q is for Quanta, L is for other customer) EE portion 1. page 13 : Remove R42 2. page 29 : Change NET name from EN_USB_A_5V to USB_A_5V_ODL Change NET name from +USB3_P4_VBUS to PPVAR_USB_CL_VBUS U16 change from P58751BQFN52GTR-A3 to ANX7447QN-A Add R9122 U25 change from NXSP3290UK to SY6863BS5ABC 3. page 9 : Remove R931_R932_R933_R934_C7817 & R934 4. page 10 : UCLAU13 Change connect from PP3300_DSW to PCH_BATLOW# 5. page 12 : UCLK20 & K21 Change connect to PP1000_VCCSTU UCLAM40 Change connect to PP1200_VDDQ_SOC 6. page 13 : UCLAH19 Change connect to PP1800_A UCLA017 AD18 & AJ17 Change connect to PP3300_DSW UCLAD15 Change connect to PP3300_SOC_A 7. page 28 : R994 Change connect to PMOS Add R9119 U24 change from NXSP3290UK to SY6863BS5ABC 8. page 11 : R994 Change connect to PMOS 9. page 27 : Correct wifi sch.. 10. page 31 : Q64 & Q169 Could we replace 3906 transistors by 3904 transistors? These two parts are substitute component in datasheet. 11. page 25 : Unstuff R6061_R6064 & R6077 12. page 7 :Correct memory sch..			
		1C	EE portion 1. page 29 : add R9218, R9220, R9221, R9222, C7866, C7867 2. page 29 : change G sensor VDD to PP3300_A 3. page 28 : add R9219 4. page 21 : unstuff R628, R645 5. page 8 : unstuff Q167, Q168 Sch_Rev:1C_0130			
		1D	1. page 8 : Add GPIO signal for LPDDR3 detection. Add pull up and pull down with GPP_E15. And unstuff pulldown 2. page 22 : Follow reference schematic ,delete pin 39 as WARM_RESET# 3. page 25 : Modify from NVME to eMMC schematic. 4. page 32 : Unstuff C7867 R9222 & R9221 5. page 30 : Unstuff Q170 6. page 31 : Unstuff R9073 , stuff R9072 7. page 36 : Unstuff R9106 & R9107 Sch_Rev:1D			
		1E	1. Page 8 : 1. Add net name : PCH_EMMC_CONFIG 2. R9251 & R9252 Change to 10K PU. 3. Add table. 4. Stuff R9002 2. Page 32 : Unstuff R9239 and R9123 3. Page 53 : 1. DSX@ (PRC52_PCC76 & PCC73) change to stuff 2. DSX_S0X@ (PRC27 & PCC77) change to stuff 3. MP@ (PRC26_PRC266_PRC25 & PRC51) change to stuff 4. XDP@ (R233_R236_R235 & R238) change to stuff 5. NDSX@ (PRC60_PRC55_PRC56 & PRC58) change to unstuff 6. Remove PUCS related parts & circuit. 4. Page 10 : Del DDR Debug (Remove R24 & R48) 5. Page 31 : Add level shift (Q50 & Q171) 6. Page 39 : Keep layout and update DNA address information 7. Page 13 : Connect GPP_E1 to PEN_EJECT_ODL 8. Page 21 : Correct part number for U4. Change part number to W25Q128JVSIM 9. Page 22 : Unstuff R9250 and stuff R9249 10. Page 30 : Stuff Q170 11. Page 24 : Revised U103 related parts & circuit. 12. Page 28 : R338 & R5286 connect to PP3300_S_TOUCHSCREEN			
		2A	EE portion 1. Page 36 : Add R79033 ohm 1 & C785(180pf) for ESD 2. Page 13 & 15 : Add C7888 & C7889 (100nF) filter for enhance sensitive net ESD level 3. Page 24 : R401 change to 2.2 ohm for ESD 4. Page 24 : TOUCHSCREEN_DSW not need to connect to the panel side. 5. Page 13 : Follow reference schematic to add_R9265 6. Page 8 : Change R9251 to 1K ohm. 7. Page 25 : WARM_RESET# PU 100K ohm to PP3300_A PWR portion 1. Page 40 : Stuff PR960 with 0 ohm for wrong strapping resistor 3. Page 42 : Add PR4976 and PR4977 with 0 ohm for measure 4. Page 43 : PC28,PC29 change to 0402 package 5. Page 44 : PR105 change pull high to PP1000_VCCST 6. Page 46 : Change PR906/PR918/PR924 location from beofore Divided resistor to After output MLCCs. 7. Page 47 : Make option table for U22 and U42 8. Page 53 : PCC77 change to 56p to meet S0x sequence 9. Page 45 : Add PR188 10. Page 44 : Unstuff PR110 11. Page 45 : PR127 & PR929 change to 0.01 ohm 12. Page 45 : Add PRC27_PUC8_PRC233 & PRC232 for power sequence adjustment			
		2B	1. Page 37 : Reverse CN18 for design change. 2. Page 28 : Change DMIC level shifter to FJA158KAVCS(b) 1.1 max (TXB0302QDMR: Waiting for vender spec for apply P/N & footprint.) 3. Page 16 : Follow Ined review to remove TP11, TP12 & TP6 4. Page 23 : Stuff R678 and R677 5. Page 32 : USB_C1_SBU1 & USB_C1_SBU2 add related circuit. 6. Page 31 : GYRO change power source to PP3300_DSW 7. Page 17 : ADD PP3300_DSW to J10.37 for G sensor 8. Page 31 : ADD PP1800_A to J10.13 for EMR 9. Page 32 : Stuff R9123 10. Page 25 & 46 : PP1100_S_NVME rename to PP1200_S_NVME 11. Page 24 : Add PRC233 for power sequence adjustment 12. Page 16 : Follow Ined review that PPVAR_GTX_VCC change to PPVAR_VCC, and always stuff R6016 & R21			
		2C	1. Page 28 : Unstuff R9006_R9007_Q165 & Q166 and stuff R9215 & R9216 2. Page 24 : Reverse R9268. PWR portion 1. Page 40 : Change PC28 & PC29 from 1uF to 2.2uF 2. Page 40 : Unstuff PR385 and stuff PR960 3. Page 54 : PP3300_S INA is on the wrong address it should be on tx49			
		2D	1. Page 52 : Replace PU901 with TPS62125 .			
		2E	1. Page 35 : Add R9269. 2. Page 24 : Add R9270. 3. Page 40 : Add PR4978 & PR4979 Change PU53 to TPS22915			
DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	
<div><div><div>Quanta Computer Inc. PROJECT : SEA</div></div><div><div>1:1 Change list</div></div></div>						

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